The PNP/5280 BDM Signals

The PNP/5280 PGA-169 pinout offers a BDM (Background Debug Modus) interface for debug and real-time trace. This interface allows also the on-board Flash chip programming.

Pin	Name	Function	BDM Connector Pin
---	VCC	Connected to 3.3 VDC	1
---	GND	Connected to Ground	2
E15	TA#	Transfer Acknowledge	3
A5	BKPT#	BDM Breakpoint	4
L16	Reset#	CPU Reset Input	5
A7	DSCLK	BDM Development Serial Clock	6
A6	DSI	BDM Development Serial Input	7
B5	TCLK	Test Clock Input	8
K17	PST3	Processor Status Bit 3	9
B6	DSO	BDM Development Serial Output	10
J17	PST2	Processor Status Bit 2	11
K16	DDATA3	Debug Data Bit 3	12
H17	PST1	Processor Status Bit 1	13
J16	DDATA2	Debug Data Bit 2	14
G17	PST0	Processor Status Bit 0	15
H16	DDATA1	Debug Data Bit 1	16
L17	PSTCLK	CPU Clock Output	17
G16	DDATA0	Debug Data Bit 0	18
---	---	Pulled down to Ground with 1K	19
C5	RCM	Remote Console Mode	20

Table 1: PNP/5280 BDM Signals