The PNP/5280 Pinout

The 169 pins of the PGA socket are associated to 17 lines and 17 columns. The individual lines are allocated to digits; letters localizes the columns.

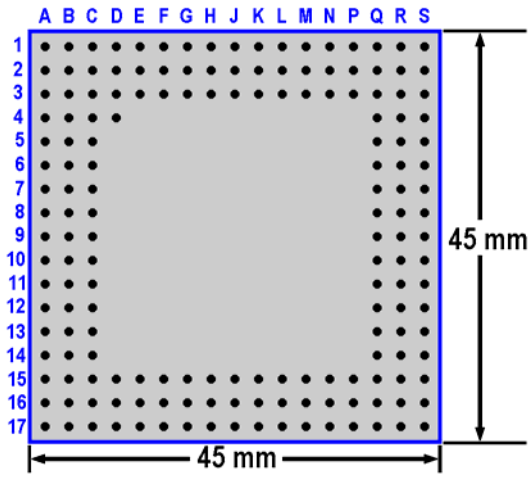

Fig. 1: PNP/5280 Pin Side View

The following tables 1-17 show the pinout of the PNP/5280. Please consider, that the notation of letters is not continuous. The letters „I“ and „O“ are not be provided. These columns are not available.

Pin	Name	Function
A1	RX1-	Ethernet LAN1 Interface, RX-
A2	TX1-	Ethernet LAN1 Interface, TX-
A3	RX2-	Ethernet LAN2 Interface, RX-
A4	TX2-	Ethernet LAN2 Interface, TX-
A5	BKPT#	BDM Interface Function
A6	DSI	BDM Interface Function
A7	DSCLK	BDM Interface Function
A8	Fix0	This Pin is always ‘0’ (internal connected to GND)
A9	SA22	Expansion Bus, Address Bit 22
A10	SA20	Expansion Bus, Address Bit 20
A11	SA18	Expansion Bus, Address Bit 18
A12	SA16	Expansion Bus, Address Bit 16
A13	SA13	Expansion Bus, Address Bit 13
A14	SA10	Expansion Bus, Address Bit 10
A15	SA8	Expansion Bus, Address Bit 8
A16	SA7	Expansion Bus, Address Bit 7
A17	SA6	Expansion Bus, Address Bit 6

Table 1: Pins A1 to A17

Pin	Name	Function
B1	RX1+	Ethernet LAN1 Interface, RX+
B2	TX1+	Ethernet LAN1 Interface, TX+
B3	RX2+	Ethernet LAN2 Interface, RX+
B4	TX2+	Ethernet LAN2 Interface, TX+
B5	TCLK	BDM Interface Function
B6	DSO	BDM Interface Function
B7	Fix0	This Pin is always ‘0’ (internal connected to GND)
B8	SA23	Expansion Bus, Address Bit 23
B9	SA21	Expansion Bus, Address Bit 21
B10	SA19	Expansion Bus, Address Bit 19
B11	SA17	Expansion Bus, Address Bit 17
B12	SA15	Expansion Bus, Address Bit 15
B13	SA12	Expansion Bus, Address Bit 12
B14	SA9	Expansion Bus, Address Bit 9
B15	SA5	Expansion Bus, Address Bit 5
B16	SA3	Expansion Bus, Address Bit 3
B17	SA4	Expansion Bus, Address Bit 4

Table 2: Pins B1 to B17

Pin	Name	Function
C1	TXD1	COM1 Serial Port, TXD Pin
C2	RXD1	COM1 Serial Port, RXD Pin
C3	VBAT	Real Time Clock Battery Input
C4	GND	Ground
C5	RCME	Remote Console Mode Enable (Low-active)
C6	VCC	3.3 Volt Power Input
C7	GND	Ground
C8	GND	Ground
C9	GND	Ground
C10	GND	Ground
C11	GND	Ground
C12	VCC	3.3 Volt Power Input
C13	SA14	Expansion Bus, Address Bit 14
C14	SA11	Expansion Bus, Address Bit 11
C15	SA2	Expansion Bus, Address Bit 2
C16	SA0	Expansion Bus, Address Bit 0
C17	SA1	Expansion Bus, Address Bit 1

Table 3: Pins C1 to C17

Pin	Name	Function
D1	TXD2	COM2 Serial Port, TXD Pin
D2	RXD2	COM2 Serial Port, RXD Pin
D3	GND	Ground
D4	GND	Ground
D15	CS3	Chip Select Output 3 (Low-active)
D16	CS1	Chip Select Output 1 (Low-active)
D17	CS2	Chip Select Output 2 (Low-active)

Table 4: Pins D1 to D17

Pin	Name	Function
E1	ERXD2	MII Receive Data Bit 2
E2	ERXD3	MII Receive Data Bit 3
E3	LAN1.LED	Activity LED Ethernet LAN1 Interface
E15	RDY / TA#	External Ready Input / BDM Interface Function
E16	CS4	Chip Select Output 4 (Low-active)
E17	CS5	Chip Select Output 5 (Low-active)

Table 5: Pins E1 to E17

Pin	Name	Function
F1	ERXD0	MII Receive Data Bit 0
F2	ERXD1	MII Receive Data Bit 1
F3	VCC	3.3 Volt Power Input
F15	VCC	3.3 Volt Power Input
F16	OE	Expansion Bus, Output Enable (Output - Low-active)
F17	WE	Expansion Bus, Write Enable (Output - Low-active)

Table 6: Pins F1 to F17

Pin	Name	Function
G1	ERXDV	MII Receive Data Valid
G2	ERXCLK	MII Receive Clock
G3	GND	Ground
G15	GND	Ground
G16	DDATA0	BDM Interface Function
G17	PST0	BDM Interface Function

Table 7: Pins G1 to G17

Pin	Name	Function
H1	EMDC	MII Management Data Clock
H2	ERXER	MII Receive Error
H3	GND	Ground
H15	GND	Ground
H16	DDATA1	BDM Interface Function
H17	PST1	BDM Interface Function

Table 8: Pins H1 to H17

Pin	Name	Function
J1	ECRS	MII Carrier Sense
J2	ECOL	MII Collision Detect
J3	GND	Ground
J15	GND	Ground
J16	DDATA2	BDM Interface Function
J17	PST2	BDM Interface Function

Table 9: Pins J1 to J17

Pin	Name	Function
K1	EMDIO	MII Management Data I/O
K2	ETXER	MII Transmit Error
K3	GND	Ground
K15	GND	Ground
K16	DDATA3	BDM Interface Function
K17	PST3	BDM Interface Function

Table 10: Pins K1 to K17

Pin	Name	Function
L1	ETXEN	MII Transmit Enable
L2	ETXCLK	MII Transmit Clock
L3	GND	Ground
L15	GND	Ground
L16	Reset#	BDM Interface Function
L17	PSTCLK	BDM Interface Function

Table 11: Pins L1 to L17

Pin	Name	Function
M1	ETXD0	MII Transmit Data Bit 0
M2	ETXD1	MII Transmit Data Bit 1
M3	VCC	3.3 Volt Power Input
M15	VCC	3.3 Volt Power Input
M16	RD/WR	Read/Write Signal (Output - Write is Low-active)
M17	INT1	Interrupt Input 1

Table 12: Pins M1 to M17

Pin	Name	Function
N1	ETXD2	MII Transmit Data Bit 2
N2	ETXD3	MII Transmit Data Bit 3
N3	LAN2.LED	Activity LED Ethernet LAN2 Interface
N15	CLKOUT	Clock Output
N16	RESIN	RESET Input (Low-active)
N17	RESOUT	RESET Output (Low-active)

Table 13: Pins N1 to N17

Pin	Name	Function
P1	PC2	Parallel I/O, Port C, Bit 2
P2	PC1	Parallel I/O, Port C, Bit 1
P3	PC3	Parallel I/O, Port C, Bit 3
P15	SD2	Expansion Bus, Data Bit 2
P16	SD0	Expansion Bus, Data Bit 0
P17	SD1	Expansion Bus, Data Bit 1

Table 14: Pins P1 to P17

Pin	Name	Function
Q1	PC0	Parallel I/O, Port C, Bit 0
Q2	PB2	Parallel I/O, Port B, Bit 2
Q3	PB5	Parallel I/O, Port B, Bit 5
Q4	PA5	Parallel I/O, Port A, Bit 5
Q5	PA2	Parallel I/O, Port A, Bit 2
Q6	VCC	3.3 Volt Power Input
Q7	GND	Ground
Q8	GND	Ground
Q9	GND	Ground
Q10	GND	Ground
Q11	GND	Ground
Q12	VCC	3.3 Volt Power Input
Q13	SD17	Expansion Bus, Data Bit 17
Q14	SD14	Expansion Bus, Data Bit 14
Q15	SD5	Expansion Bus, Data Bit 5
Q16	SD3	Expansion Bus, Data Bit 3
Q17	SD4	Expansion Bus, Data Bit 4

Table 15: Pins Q1 to Q17

Pin	Name	Function
R1	PB0	Parallel I/O, Port B, Bit 0
R2	PB4	Parallel I/O, Port B, Bit 4
R3	PB7	Parallel I/O, Port B, Bit 7
R4	PA3	Parallel I/O, Port A, Bit 3
R5	PA0	Parallel I/O, Port A, Bit 0
R6	SD30	Expansion Bus, Data Bit 30
R7	SD28	Expansion Bus, Data Bit 28
R8	SD26	Expansion Bus, Data Bit 26
R9	SD24	Expansion Bus, Data Bit 24
R10	SD22	Expansion Bus, Data Bit 22
R11	SD20	Expansion Bus, Data Bit 20
R12	SD18	Expansion Bus, Data Bit 18
R13	SD15	Expansion Bus, Data Bit 15
R14	SD12	Expansion Bus, Data Bit 12
R15	SD8	Expansion Bus, Data Bit 8
R16	SD6	Expansion Bus, Data Bit 6
R17	SD7	Expansion Bus, Data Bit 7

Table 16: Pins R1 to R17

Pin	Name	Function
S1	PB1	Parallel I/O, Port B, Bit 1
S2	PB3	Parallel I/O, Port B, Bit 3
S3	PB6	Parallel I/O, Port B, Bit 6
S4	PA4	Parallel I/O, Port A, Bit 4
S5	PA1	Parallel I/O, Port A, Bit 1
S6	SD31	Expansion Bus, Data Bit 31
S7	SD29	Expansion Bus, Data Bit 29
S8	SD27	Expansion Bus, Data Bit 27
S9	SD25	Expansion Bus, Data Bit 25
S10	SD23	Expansion Bus, Data Bit 23
S11	SD21	Expansion Bus, Data Bit 21
S12	SD19	Expansion Bus, Data Bit 19
S13	SD16	Expansion Bus, Data Bit 16
S14	SD13	Expansion Bus, Data Bit 13
S15	SD11	Expansion Bus, Data Bit 11
S16	SD10	Expansion Bus, Data Bit 10
S17	SD9	Expansion Bus, Data Bit 9

Table 17: Pins S1 to S17

Document History

Revision	Date		Name
1.00	01.07.2004	First Version.	KDW
1.01	12.08.2004	LAN2, MII Pins and Fix0 Pins added	KDW
1.02	02.05.2005	BDM Signals added	KDW