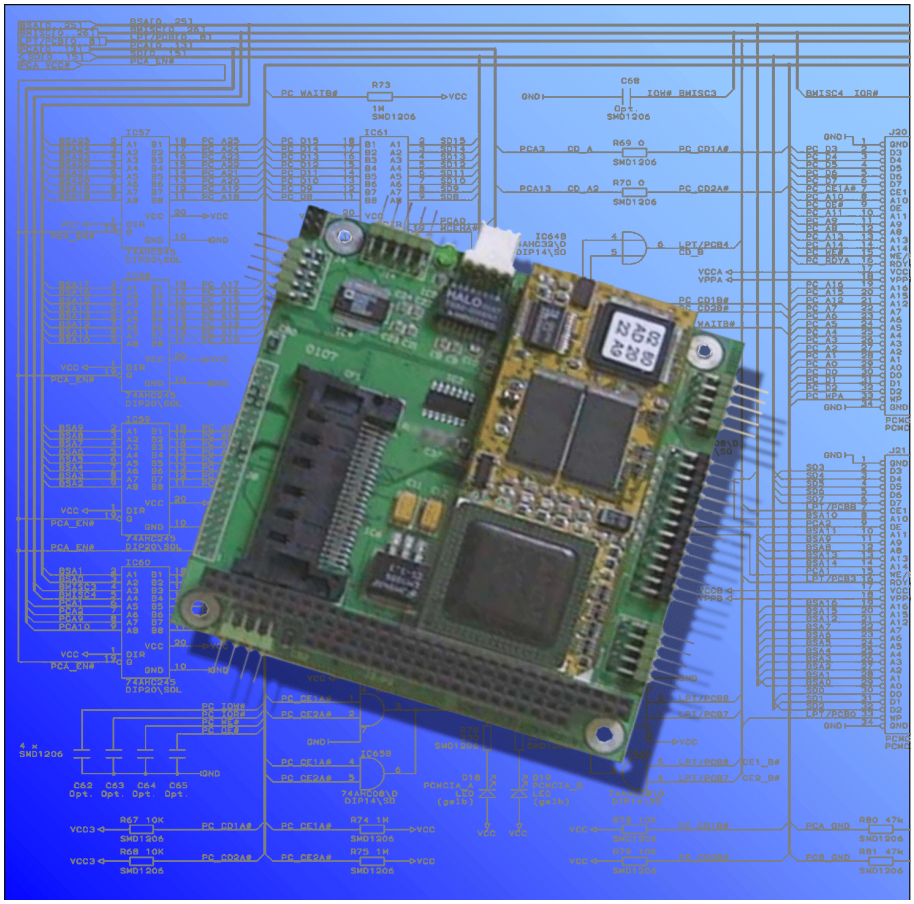
CP/486SX2



PC/104 Single Board Computer

User´s Manual

Content

List of Figures

List of Tables

1. Introduction

The ***CP/486SX2*** provides a complete high performace 32-bit PC/AT-based embedded single board computer (SBC) in a ultra compact PC/104 form factor (90 * 96 mm / 3.6 * 3.8"). The ***CP/486SX2*** includes all standard motherboard functions plus 8- or 16- Mbyte DRAM, bootable FLASH Disk with up to 4 Mbyte, two serial ports, one parallel port, one NE2000 10BASE-T Ethernet networking interface, one Compact Flash Adapter and (E)IDE hard disk interface.The ***CP/486SX2*** is an ideal platform for bridging existing equipment to Ethernet networks.

1.1 Technical Data

- Two RS232C serial ports (COM1/COM2)
- One parallel port with SPP-, EPP-, ECP- modes
- Optional Enhanced IDE-Interface for two devices
- One Compact FLASH Adapter
- 10 Mbps 10BASE-T Interface
- 4-pin LAN-connector
- Bootoption for NE2000 FLASH
- LED for RxD(ata)/ LAN-activity
- Speaker port, 0.1 watt drive
- Remote Console Mode
- Standard 16-bit PC/104 Interface
- Standard PC/104 size 90 * 96 mm
- Only +5 VDC (+- 5%) power
- Operating Temperatur 0° to +60° C
- Storage Temperature -55° to +85° C
- 10% to 90% relative humidy, non condensing
- 600 mA current by use of ADNP-33 MHz

1.2 Installation Instruction

Static electricity can seriously damage your component. Please ensure that you have discharged any static electricity by grounding yourself before you begin.

2. Layout

The following figure in this chapter will give you an overview of the available interfaces and their position on the ***CP/486SX2***.

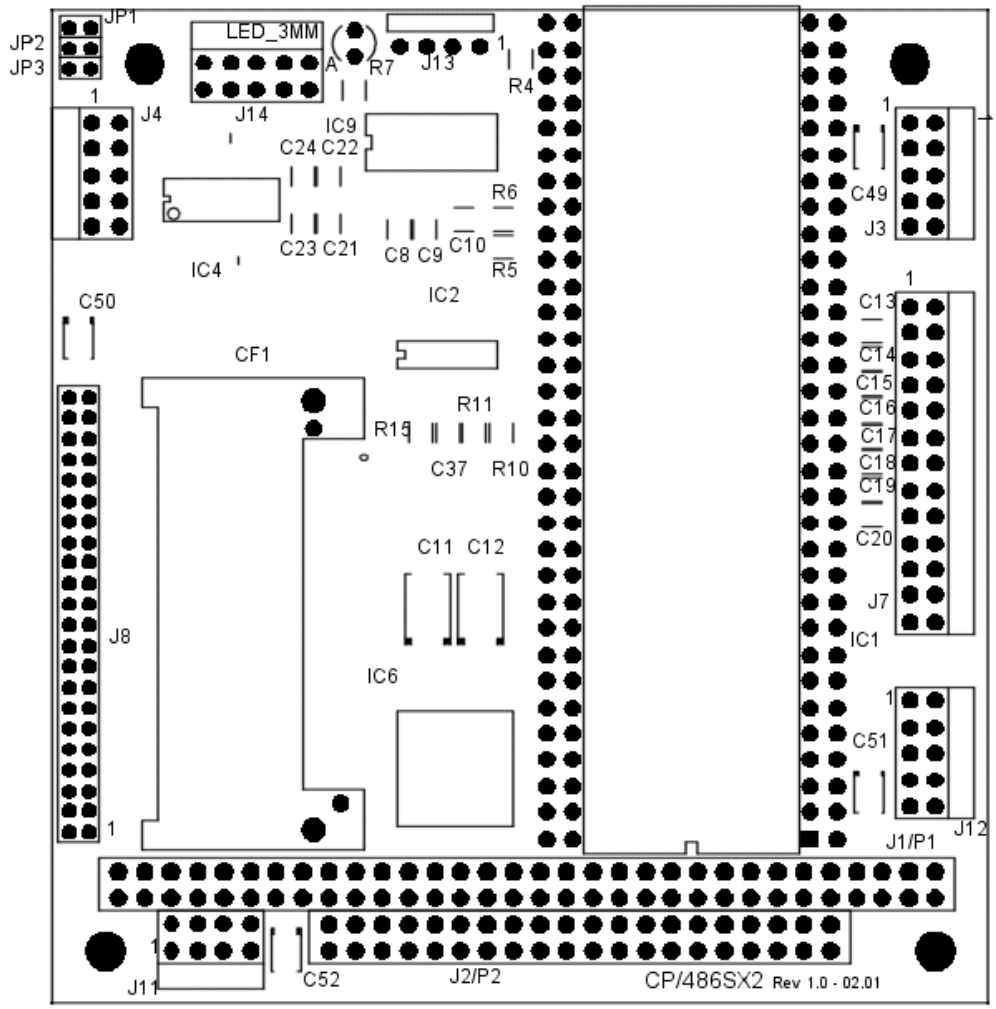


Figure 1: Board Layout

3. Jumper

The ***CP/486SX2*** is equipped with a 6-pin jumper field to use for system-setup settings. By that you are able to activate or deactivate the Remote Console Mode and/or the FLASH BIOS Hardware Lock

3.1 The Configuration Jumper JP1

The following figure shows you the position of the jumper JP1 on the ***CP/486SX2***.

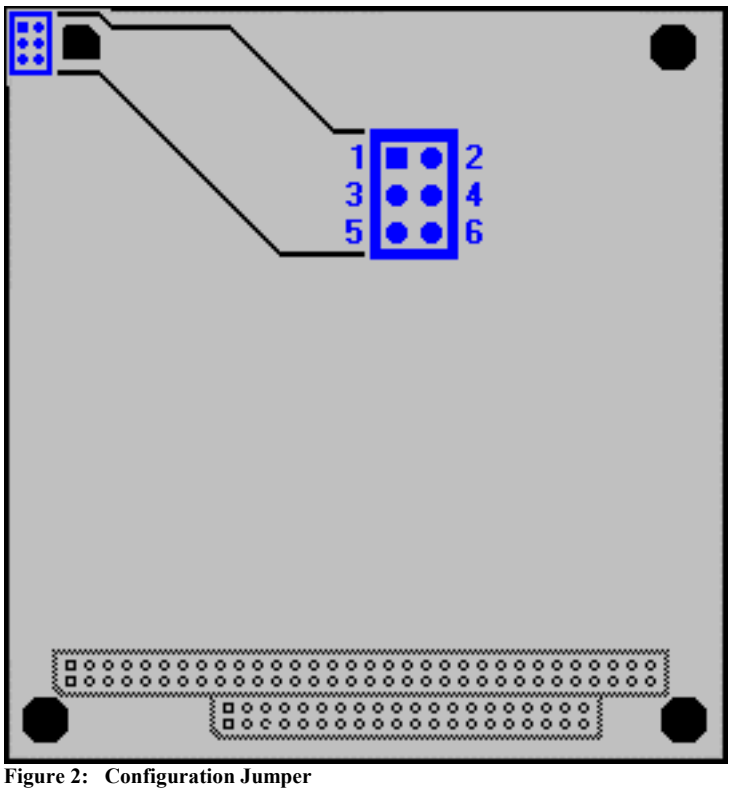


Figure 2: Configuration Jumper

The following table shows the possible settings.

Jumper Position	Status	Function
Pin 1 – 2	open	reserved
Pin 1 – 2	closed	reserved
Pin 3 – 4	open	Remote Console Mode (RCM) deactivated
Pin 3 – 4	closed	Remote Console Mode (RCM) activated
Pin 5 – 6	open	FLASH BIOS Hardware Lock activated
Pin 5 – 6	closed	FLASH BIOS Hardware Lock deactivated

Table 1: Jumper JP1

4. Connectors

The following figure shows the position of the Connectors on the ***CP/486SX2***.

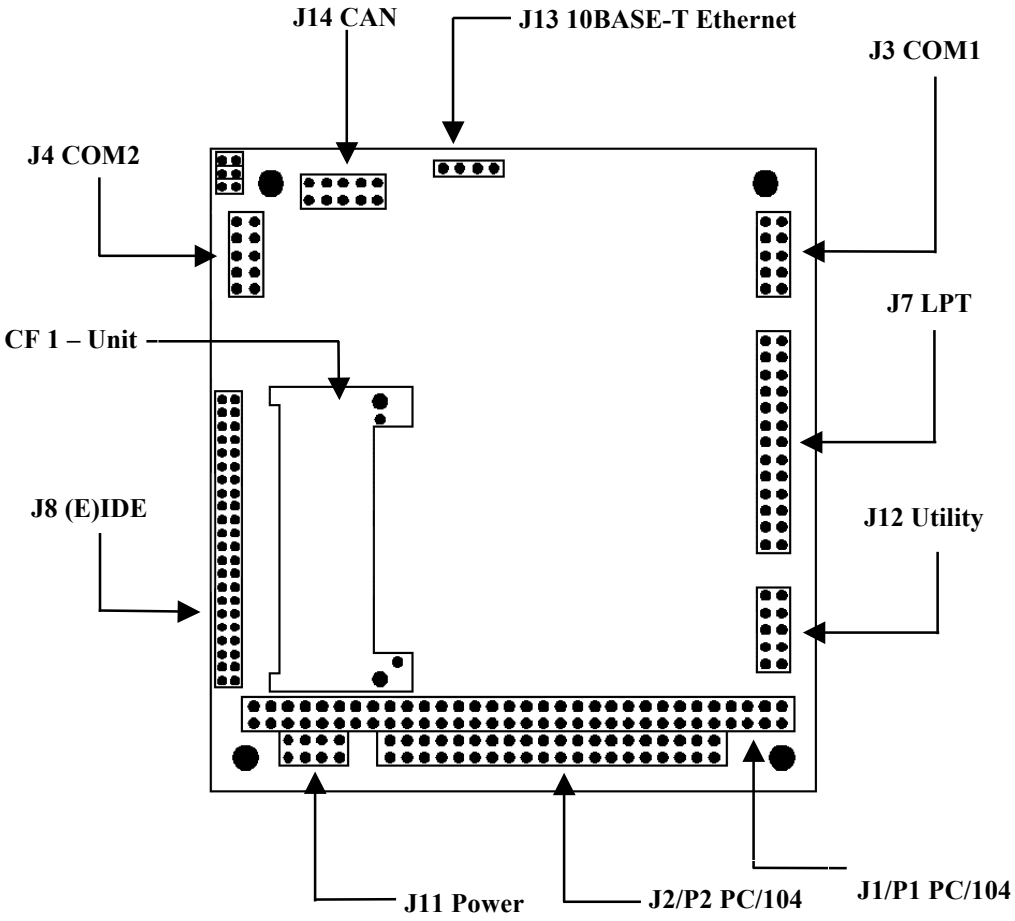


Figure 3: Connector Overview

4.1 The PC/104-Interface J1/P1

The J1/P1connector forms the 8 bit PC/104 bus. The extension onto a 16 bit PC/104 bus occurs by the connector J2/P2.

The figure shows the position of the PC/104 Interface which is called J1/P1.

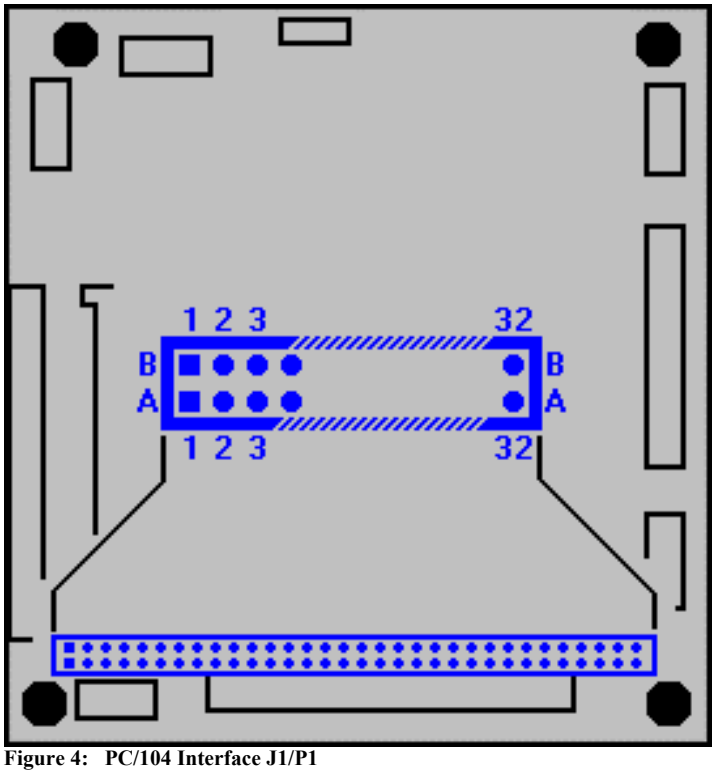


Figure 4: PC/104 Interface J1/P1

The table shows the assignment of the pins A1 to A32 from the PC/104 interface J1/P1.

Pin	Name	Function	IN/OUT
A1	IOCHK#	Bus NMI Input	IN
A2	SD7	Data Bit 7	I/O
A3	SD6	Data Bit 6	I/O
A4	SD5	Data Bit 5	I/O
A5	SD4	Data Bit 4	I/O
A6	SD3	Data Bit 3	I/O
A7	SD2	Data Bit 2	I/O
A8	SD1	Data Bit 1	I/O
A9	SD0	Data Bit 0	I/O
A10	IOCHRDY	Processor Ready Ctrl	IN
A11	AEN	Address Enable	I/O
A12	SA19	Address Bit 19	I/O
A13	SA18	Address Bit 18	I/O
A14	SA17	Address Bit 17	I/O
A15	SA16	Address Bit 16	I/O
A16	SA15	Address Bit 15	I/O
A17	SA14	Address Bit 14	I/O
A18	SA13	Address Bit 13	I/O
A19	SA12	Address Bit 12	I/O
A20	SA11	Address Bit 11	I/O
A21	SA10	Address Bit 10	I/O
A22	SA9	Address Bit 9	I/O
A23	SA8	Address Bit 8	I/O
A24	SA7	Address Bit 7	I/O
A25	SA6	Address Bit 6	I/O
A26	SA5	Address Bit 5	I/O
A27	SA4	Address Bit 4	I/O
A28	SA3	Address Bit 3	I/O
A29	SA2	Address Bit 2	I/O
A30	SA1	Address Bit 1	I/O
A31	SA0	Address Bit 0	I/O
A32	GND	Ground	N/A

Table 2: J1/P1 pin assignment A1 to A32

The table shows the assignment of the pins B1 to B32 from the PC/104-interface J1/P1.

Pin	Name	Function	IN/OUT
B1	GND	Ground	N/A
B2	RESETDRV	System Reset Signal	OUT
B3	+5 VDC	+5 Volt Power	N/A
B4	IRQ9	Interrupt Request 9	IN
B5	-5 VDC	-5 Volt Power	N/A
B6	DRQ2	DMA Request 2	IN
B7	-12 VDC	-12 Volt Power	N/A
B8	ENDXFR#	Zero Wait State	IN
B9	+12 VDC	+12 Volt Power	N/A
B10	NC	N/A	N/A
B11	SMEMW#	Memory Write (first MB)	I/O
B12	SMEMR#	Memory Read (first MB)	I/O
B13	IOW#	I/O Write	I/O
B14	IOR#	I/O Read	I/O
B15	DACK3#	DMA Acknowledge 3	OUT
B16	DRQ3	DMA Request 3	IN
B17	DACK1#	DMA Acknowledge 1	OUT
B18	DRQ1	DMA Request 1	IN
B19	REFRESH#	Memory Refresh	I/O
B20	SYSCLK	System Clock (e.g. 8 MHz)	OUT
B21	IRQ7	Interrupt Request 7	IN
B22	IRQ6	Interrupt Request 6	IN
B23	IRQ5	Interrupt Request 5	IN
B24	IRQ4	Interrupt Request 4	IN
B25	IRQ3	Interrupt Request 3	IN
B26	DACK2#	DMA Acknowledge 2	OUT
B27	TC	DMA Terminal Count	OUT
B28	BALE	Address Latch Enable	OUT
B29	+5 VDC	+5 Volt Power	N/A
B30	OSC	14.3 MHz Clock	OUT
B31	GND	Ground	N/A
B32	GND	Ground	N/A

Table 3: J1/P1 pin assignement B1 to B32

4.2 The PC/104-Interface J2/P2

The figure shows the position of the PC/104 interface J2/P2.

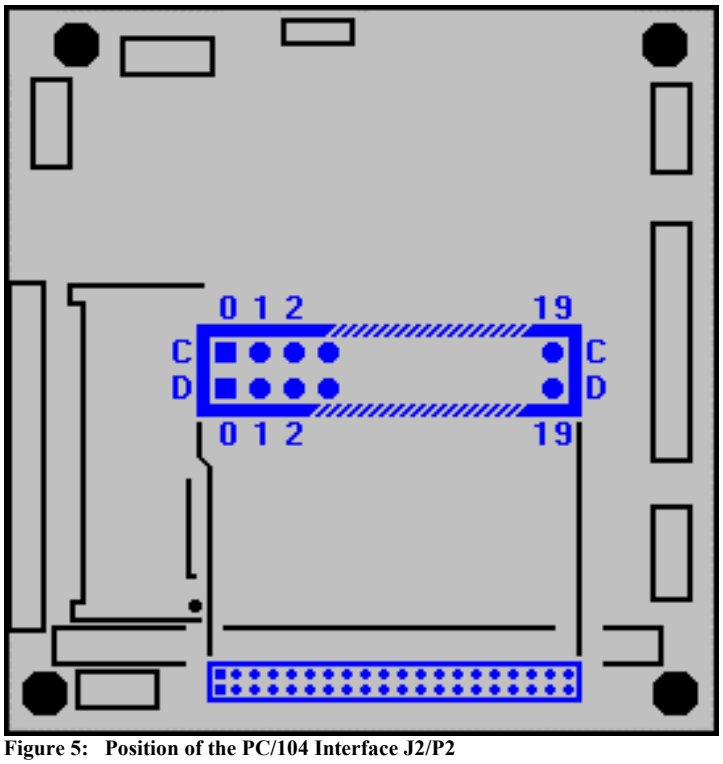


Figure 5: Position of the PC/104 Interface J2/P2

The table shows the pin assignments of the pins C0 to C19 of the PC/104-interface J2/P2.

Pin	Name	Function	IN/OUT
C0	GND	Ground	N/A
C1	SBHE#	Bus High Enable	I/O
C2	LA23	Address Bit 23	I/O
C3	LA22	Address Bit 22	I/O
C4	LA21	Address Bit 21	I/O
C5	LA20	Address Bit 20	I/O
C6	LA19	Address Bit 19	I/O
C7	LA18	Address Bit 18	I/O
C8	LA17	Address Bit 17	I/O
C9	MEMR#	Memory Read	I/O
C10	MEMW#	Memory Write	I/O
C11	SD8	Data Bit 8	I/O
C12	SD9	Data Bit 9	I/O
C13	SD10	Data Bit 10	I/O
C14	SD11	Data Bit 11	I/O
C15	SD12	Data Bit 12	I/O
C16	SD13	Data Bit 13	I/O
C17	SD14	Data Bit 14	I/O
C18	SD15	Data Bit 15	I/O
C19	GND	Ground	N/A

Table 4: J2/P2 pin assignment C0 to C19

The table shows the assignment of the pins D0 to D19 of the PC/104 interface J2/P2.

Pin	Name	Function	IN/OUT
D0	GND	Ground	N/A
D1	MEMCS16#	16 Bit Memory Access	IN
D2	IOCS16#	16 Bit I/O Access	IN
D3	IRQ10	Interrupt Request 10	IN
D4	IRQ11	Interrupt Request 11	IN
D5	IRQ12	Interrupt Request 12	IN
D6	IRQ15	Interrupt Request 15	IN
D7	IRQ14	Interrupt Request 14	IN
D8	DACK0#	DMA Acknowledge 0	OUT
D9	DRQ0	DMA Request 0	IN
D10	DACK5#	DMA Acknowledge 5	OUT
D11	DRQ5	DMA Request 5	IN
D12	DACK6#	DMA Acknowledge 6	OUT
D13	DRQ6	DMA Request 6	IN
D14	DACK7#	DMA Acknowledge 7	OUT
D15	DRQ7	DMA Request 7	IN
D16	+5 VDC	+5 Volt Power	N/A
D17	MASTER#	Bus Master Assert	IN
D18	GND	Ground	N/A
D19	GND	Ground	N/A

Table 5: J2/P2 pin assignment D0 to D19

4.3 The COM1-Connector J3

The ***CP/486SX2*** offers two COM interfaces, to connect the board with different peripherals. The figure shows the position of the first from two available COM interfaces, COM1, on the ***CP/486SX2***.

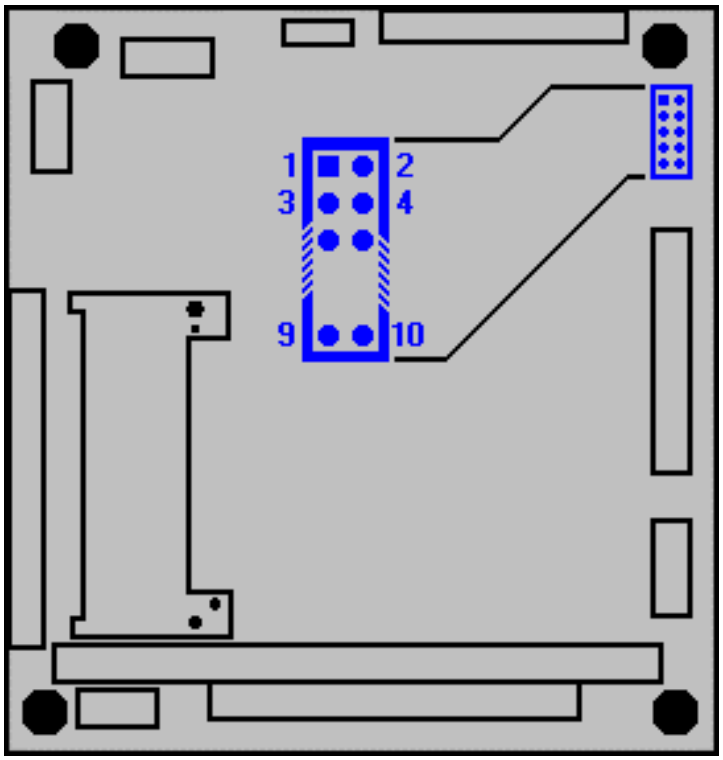


Figure 6: Position of the COM1 Interface J3

The table shows the assignment from pin 1 to 10 of the COM1 interface J3.

Pin	Name	Function	IN/OUT
1	DCD	Data Carrier Detect	IN
2	DSR	Data Set Ready	IN
3	RXD	Receive Data	IN
4	RTS	Request To Send	OUT
5	TXD	Transmit Data	OUT
6	CTS	Clear To Send	IN
7	DTR	Data Terminal Ready	OUT
8	RI	Ring Indicator	IN
9	GND	Ground	N/A
10	NC	N/A	N/A

Table 6: Pin assignment of the COM1 Interface J3

4.4 The COM2-Connector J4

In addition to the COM1 interface the ***CP/486SX2*** is further equipped with a second serial COM interface. The figure shows the position of this COM2-interface on the ***CP/486SX2***.

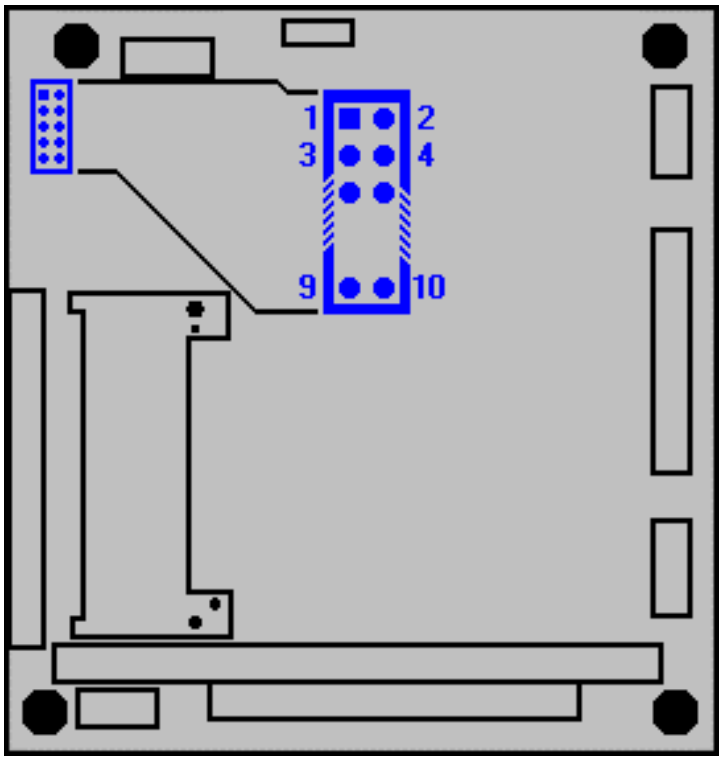


Figure 7: Position of the COM2 Interface J4

The table shows the assignment of the COM2 interface J4.

Pin	Name	Function	IN/OUT
1	DCD	Data Carrier Detect	IN
2	DSR	Data Set Ready	IN
3	RXD	Receive Data	IN
4	RTS	Request To Send	OUT
5	TXD	Transmit Data	OUT
6	CTS	Clear To Send	IN
7	DTR	Data Terminal Ready	OUT
8	RI	Ring Indicator	IN
9	GND	Ground	N/A
10	NC	N/A	N/A

Table 7: Pin assignment of the COM2 Interface J4

4.5 The LPT-Connector J7

The ***CP/486SX2*** is equipped with one parallel LPT interface. The connection to peripherals is made by the connector J7. The following figure shows the position of the LPT interface J7 on the ***CP/486SX2***.

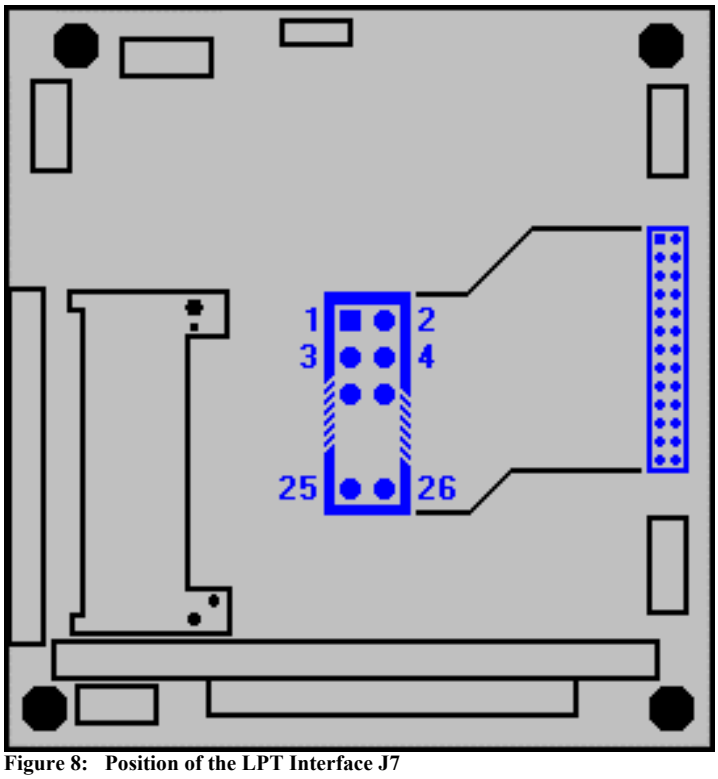


Figure 8: Position of the LPT Interface J7

The table shows the assignment of the LPT interface J7.

Pin	Name	Function	IN/OUT
1	STRB#	Output Data Strobe	OUT
2	AUTOFD#	Autofeed	OUT
3	PD0	Printer Data Bit 0 (LSB)	I/O
4	ERROR#	Printer Error	IN
5	PD1	Printer Data Bit 1	I/O
6	INIT#	Initialize Printer	OUT
7	PD2	Printer Data Bit 2	I/O
8	SLCTIN	Select Printer	OUT
9	PD3	Printer Data Bit 3	I/O
10	GND	Ground	N/A
11	PD4	Printer Data Bit 4	I/O
12	GND	Ground	N/A
13	PD5	Printer Data Bit 5	I/O
14	GND	Ground	N/A
15	PD6	Printer Data Bit 6	I/O
16	GND	Ground	N/A
17	PD7	Printer Data Bit 7 (MSB)	I/O
18	GND	Ground	N/A
19	ACK#	Character Accepted	IN

20	GND	Ground	N/A
21	BUSY	Cannot Receive Data	IN
22	GND	Ground	N/A
23	PE	Paper Empty	IN
24	GND	Ground	N/A
25	SLCTOUT	Printer Selected	IN
26	NC	N/A	N/A

Table 8: Pin assignment of the LPT Interface J7

4.6 The (E)IDE-Connector J8

The figure shows the position of the (E)IDE interface J8 on the ***CP/486SX2***.

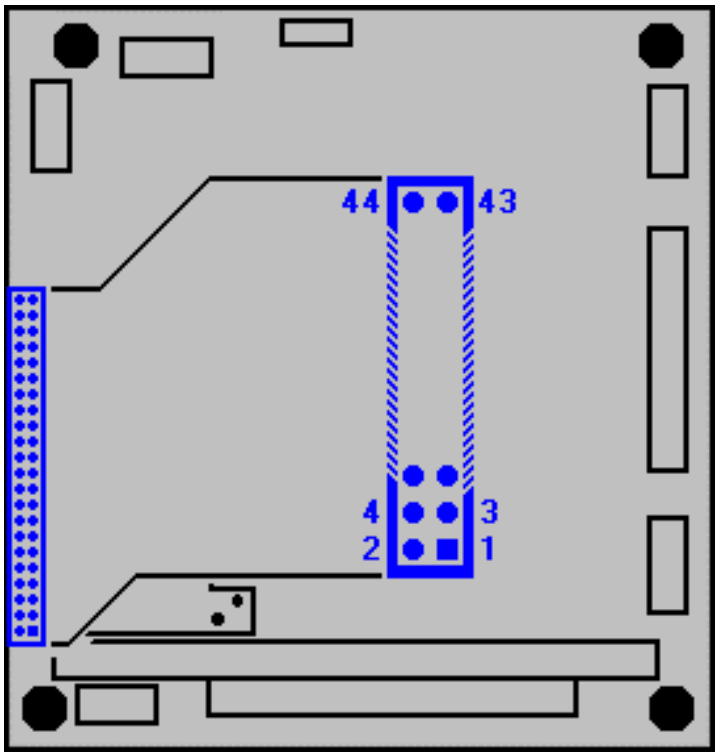


Figure 9: Position of the (E)IDE Interface J8

The table shows the assignment of the (E)IDE interface J8.

Pin	Name	Function	IN/OUT	Pin	Name	Function	IN/OUT
1	RESET#	Device Reset	OUT	23	DIOW#	Drive I/O Write	OUT
2	GND	Ground	N/A	24	GND	Ground	N/A
3	DD7	Drive Data Bit 7	I/O	25	DIOR#	Drive I/O Read	OUT
4	DD8	Drive Data Bit 8	I/O	26	GND	Ground	N/A
5	DD6	Drive Data Bit 6	I/O	27	IORDY	I/O Channel Ready	IN
6	DD9	Drive Data Bit 9	I/O	28	NC	N/A	N/A
7	DD5	Drive Data Bit 5	I/O	29	NC	N/A	N/A
8	DD10	Drive Data Bit 10	I/O	30	GND	Ground	N/A
9	DD4	Drive Data Bit 4	I/O	31	INTRQ	Drive Interrupt Req.	IN
10	DD11	Drive Data Bit 11	I/O	32	IOCS16#	Drive 16 Bit I/O	IN
11	DD3	Drive Data Bit 3	I/O	33	DA1	Drive Address Bit 1	OUT
12	DD12	Drive Data Bit 12	I/O	34	NC	N/A	N/A
13	DD2	Drive Data Bit 2	I/O	35	DA0	Drive Address Bit 0	OUT
14	DD13	Drive Data Bit 13	I/O	36	DA2	Drive Address Bit 2	OUT
15	DD1	Drive Data Bit 1	I/O	37	CS0#	Chip Select Drive 0	OUT
16	DD14	Drive Data Bit 14	I/O	38	CS1#	Chip Select Drive 1	OUT
17	DD0	Drive Data Bit 0	I/O	39	DACT#	Drive Active	IN
18	DD15	Drive Data Bit 15	I/O	40	GND	Ground	N/A
19	GND	Ground	N/A	41	+5 VDC	+5 Volt Power	N/A
20	NC	N/A	N/A	42	+5 VDC	+5 Volt Power	N/A
21	NC	N/A	N/A	43	GND	Ground	N/A
22	GND	Ground	N/A	44	NC	N/A	N/A

Table 9: Pin assignment of the (E)IDE Interface J8

4.7 The Power-Connector J11

The figure shows the position of the power-connector J11 on the ***CP/486SX2***.

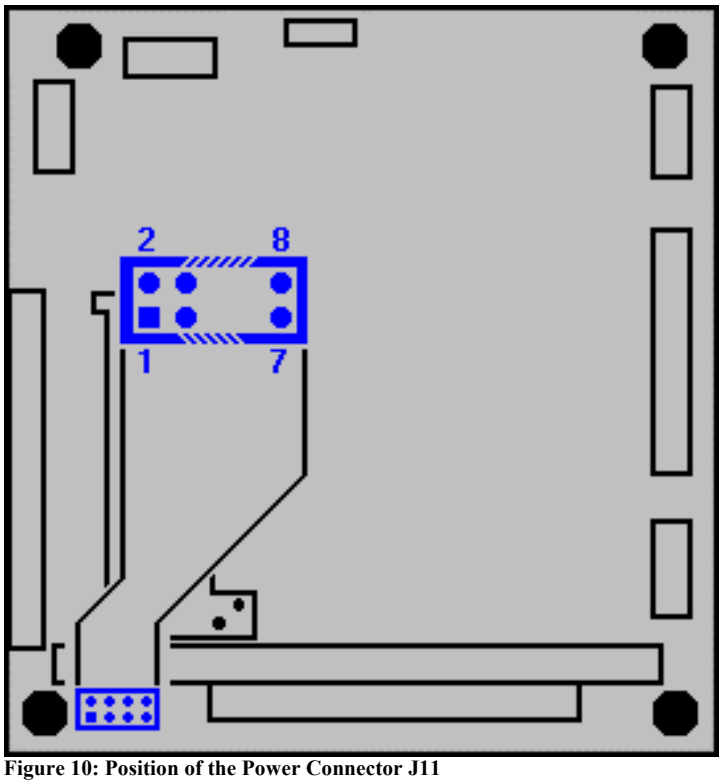


Figure 10: Position of the Power Connector J11

The table shows the assignment of the (E)IDE interface J8.

Pin	Name	Function	IN/OUT
1	GND	Ground	N/A
2	+5 VDC	+5 Volt Power Input	N/A
3	NC	N/A	N/A
4	NC	N/A	N/A
5	NC	N/A	N/A
6	NC	N/A	N/A
7	GND	Ground	N/A
8	+5 VDC	+5 Volt Power Input	N/A

Table 10: Pin assignment of the Power-Connector J11

4.8 The Utility-Connector J12

The figure shows the position of the Utility connector J12 on the ***CP/486SX2***.

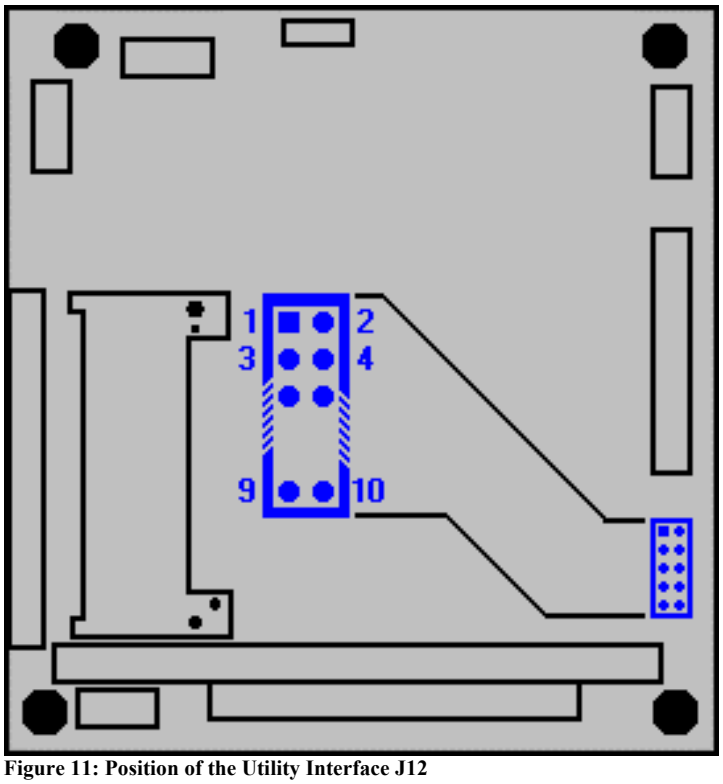


Figure 11: Position of the Utility Interface J12

The table shows the assignment of the Utility interface J12.

Pin	Name	Function	IN/OUT
1	EXTSPK	External Speaker	OUT
2	GND	Ground	N/A
3	EXTRST	External Reset Input	IN
4	KBLOCK#	Keyboard Lock	IN
5	KBDDAT	Keyboard Data	I/O
6	KBDCLK	Keyboard Clock	I/O
7	GND	Ground	N/A
8	KBDVCC	Keyboard +5 Volt Power	N/A
9	EXTBAT	External Battery Power Input	N/A
10	PWRGD	Power Good	IN

Table 11: Pin assignment of the Utility Interface J12

4.9 The 10BASE-T Ethernet-Connector J13

The figure shows the position of the 10BASE-T Ethernet interface J13.

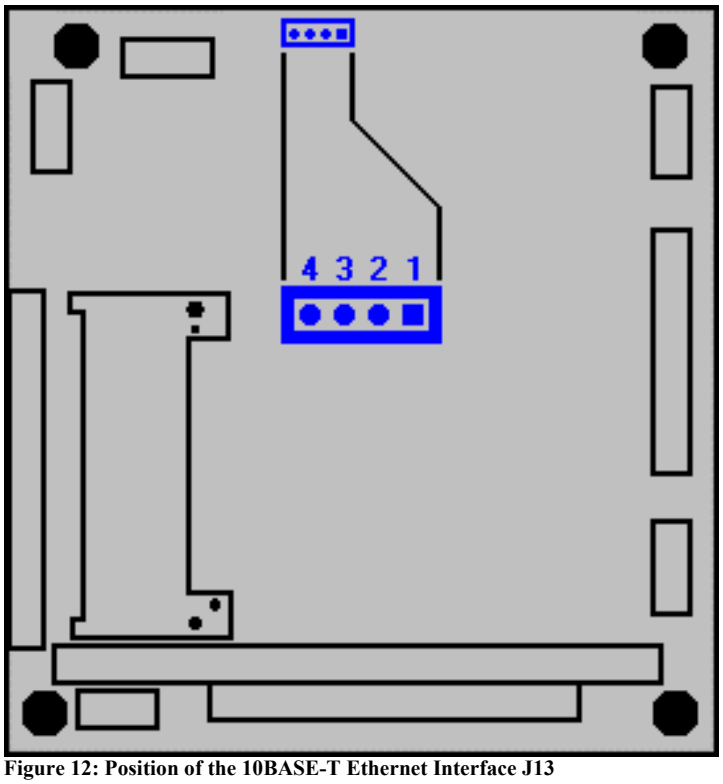


Figure 12: Position of the 10BASE-T Ethernet Interface J13

The table shows the assignment of the 10BASE-T Ethernet interface J13.

Pin	Name	Function	IN/OUT
1	TX+	10BASE-T Transmit Data Plus	OUT
2	TX-	10BASE-T Transmit Data Minus	OUT
3	RX+	10BASE-T Receive Data Plus	IN
4	RX-	10BASE-T Receive Data Minus	IN

Table 12: Pin assignment of the 10BASE-T Ethernet Interface J13

4.10 The CAN-Connector J14

The following figure shows the position of the CAN interface J14 on the ***CP/486SX2***.

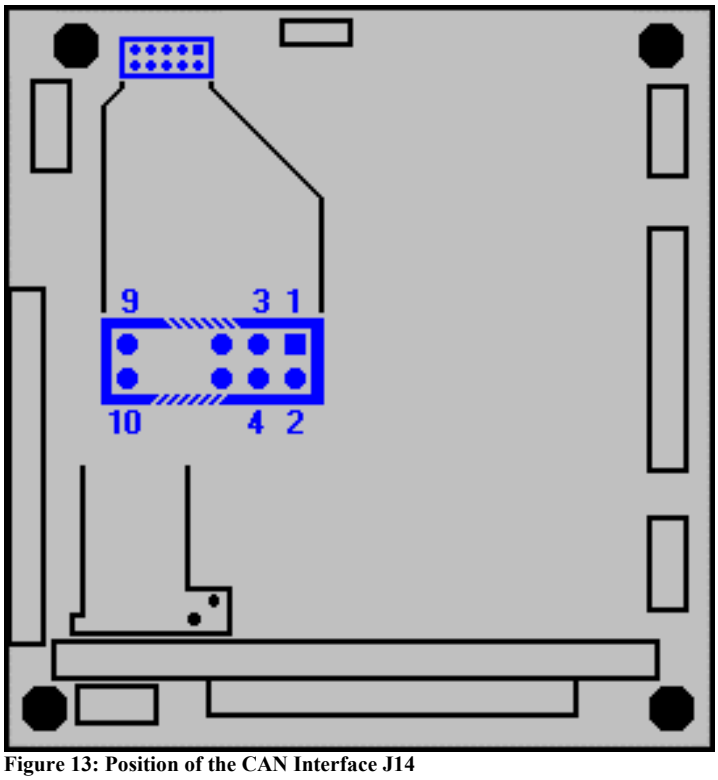


Figure 13: Position of the CAN Interface J14

The table shows the assignment of the CAN interface J14.

Pin	Name	Funktion
1	n.c.	---
2	GND	Signal Ground
3	CAN-L	Signal LOW
4	CAN-H	Signal HIGH
5	GND	Signal Ground
6	n.c.	---
7	n.c.	---
8	n.c.	---
9	n.c.	---
10	n.c.	---

Table 13: Pin assignment of the CAN Interface J14

4.11 The Compact-Flash-Unit CF1

The following figure shows the position of the Compact-Flash-Unit CF1 on the ***CP/486SX2***.

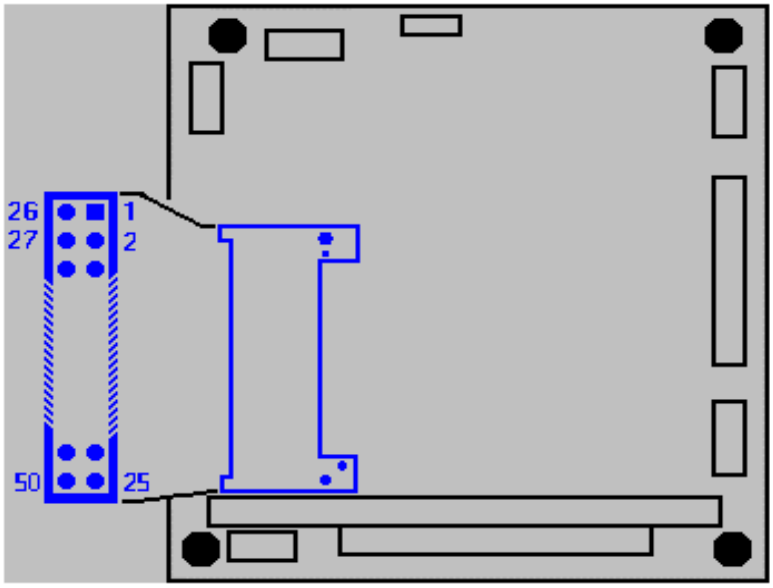


Figure 14: Position of the Compact Flash-Unit CF1

The table shows the assignment of the Compact Flash-Unit CF1.

Pin	Name	Pin	Name
1	GND	26	/CD1
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	/CS0	32	/CS1
8	A10	33	/VS1
9	/ATASEL	34	/IOR
10	A9	35	/IOW
11	A8	36	/WE
12	A7	37	IRQ
13	VCC	38	VCC
14	A6	39	/CSEL
15	A5	40	VS2
16	A4	41	RESET
17	A3	42	/WAIT
18	A2	43	/INPACK
19	A1	44	/REG
20	A0	45	/DASP
21	D0	46	/PDIAG
22	D1	47	D8
23	D2	48	D9
24	/IOCS16	49	D10
25	/CD2	50	GND

Table 14: Pin assignment of the Compact Flash-Unit CF1

5. Appendix

5.1 Jumper Information

Jumper	Function
	Jumper position open. Remove if necessary.
	Jumper position closed. Insert Jumper between pin x and pin y.

5.2 Trademark Acknowledgements

- SSV EMBEDDED SYSTEMS is a trademark of SSV GmbH.
- The SSV logo is a trademark of SSV GmbH.
- PC/104 and the PC/104 logo are trademarks of the PC/104 Consortium.
- Product names of other companies may be trademarks of their respective companies.

5.3 Disclaimer

5.4 Life Support Policy

SSV GMBH PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SSV GMBH. AS USED HEREIN.

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonable expected to result in a significant injury to the user.

- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

5.5 Technical Support

SSV Embedded Systems has an Applications Engineering staff to answer your technical questions concerning hardware, software and all kinds of system configurations. No matter if before or after you have purchased a product. Please call 49–511–40000–0, FAX 49–511–40000–40, or write your questions to the address above.

5.6 Document History

Revision	Date	Name
1.00	23.05.01	CP/486SX2. ARE

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