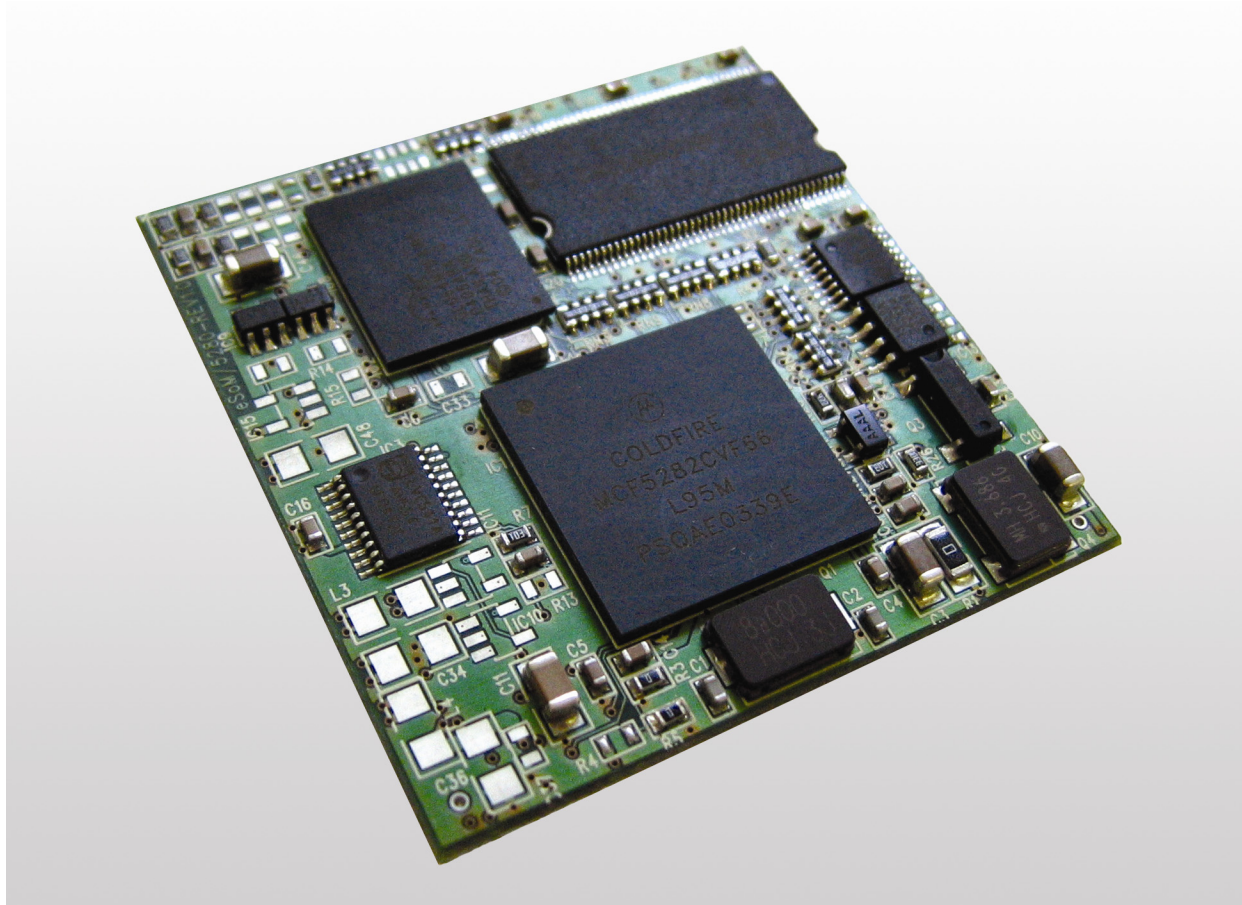


# ***PNP/5280***

## ***Board Revision 1.0***

# Hardware Reference



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Manual Revision: 1.0  
Date: 2005-05-03

# CONTENT

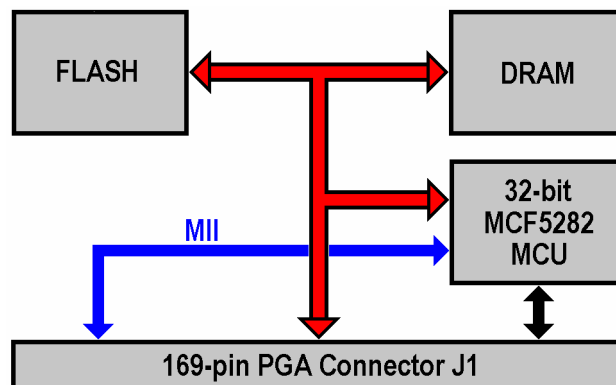
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# 1 INTRODUCTION

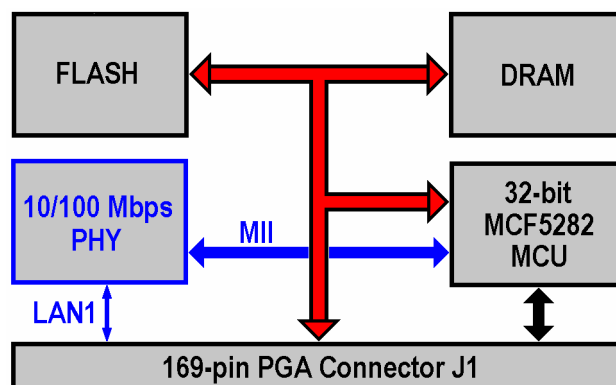
The DIL/NetPC PNP/5280 is build around Motorola's (Freescale) 32-bit ColdFire MCF5280/MCF5282 microcontroller unit (MCU) running with 66 MHz. The external main components around the ColdFire are one Flash memory chip with 8 Mbytes and one 16 MByte SDRAM memory chip. The PNP/5280 offers the footprint of a standard 169-pin PGA socket with 2.54 mm centers and all the hardware and software features necessary to add high-speed networking capabilities to any product design for industrial Ethernet applications.

The PNP/5280 is available in three different 10/100 Mbps Ethernet LAN configurations. The version with the order code **PNP/5280-M** offers the 10/100 Ethernet MII (Media Independent Interface) signals on the 169-pin PGA connector. Figure 1 shows the block diagram for this version.



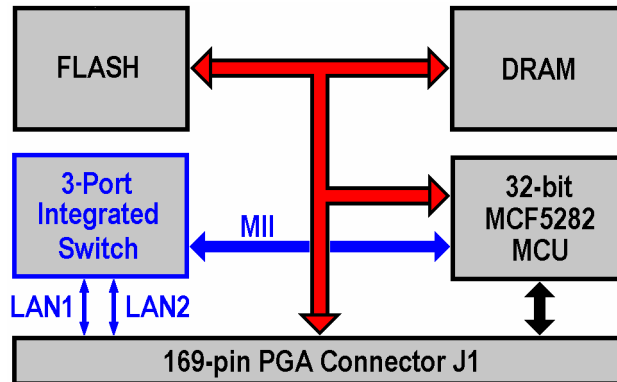
**Figure 1: Block diagram of the PNP/5280-M (PNP/5280 version with MII signals)**

With the order code **PNP/5280-N** comes a PNP/5280 version with an on-board PHY chip and one 10/100 Ethernet LAN interface. Please see the block diagram in figure 2 for more details



**Figure 2: Block diagram of the PNP/5280-N (PNP/5280 version with one LAN interface)**

The order code **PNP/5280-S** is assigned to a PNP/5280 version with a non-board 3-port integrated switch chip. Figure 3 shows the block diagram of this version. This switch chip includes two embedded PHY devices. The PNP/5280-S offers two 10/100 Ethernet LAN interfaces.



**Figure 3: Block diagram of the PNP/5280-N (PNP/5280 version with two LAN interfaces)**

The DIL/NetPC PNP/5280 is a ready-to-run full programmable 32-bit embedded networking system. The use of the PNP/5280 will allow you to realize substantial time and costs savings over other chip-based approaches. Currently, there is no other 10/100 Mbps Ethernet- and TCP/IP-based embedded networking solution with more development time savings on the market. There is also no faster Time-to-Market for your product with lower costs if 32-bit-based 10/100 Mbps Ethernet, full TCP/IP and an embedded Web server or other TCP/IP-based server software is required.

---

## 1.1 Features PNP/5280

---

- Motorola (Freescale) 32-bit MCF5280 ColdFire with 66 MHz Clock Speed
- 63 MIPS (Dhrystone 2.1)
- 16 MByte SDRAM Memory, 8 MByte FLASH Memory
- 10/100 Mbps Ethernet LAN Interface (in three different configurations)
- Two asynchronous Serial Ports
- One I2C Interchip Bus Interface
- One Queued Serial Peripheral Interface (SPI)
- One CAN Interface (Supports CAN Protocol Specification 2.0B)
- 18-bit General Purpose high-speed Parallel I/O
- 32-bit I/O Expansion Bus
- One Interrupt Input
- Five Chip Select Outputs
- Programmable General Purpose Timers and Watchdog Timer
- On-board Real Time Clock (RTC)
- RTC Backup Battery Voltage Input Pin
- Motorola BDM (Background Debug Mode) Interface for In-Circuit Debugging
- In-System Programming Features
- 169-pin JEDEC PGA Connector, 2.54 mm Centers
- 3.3 Volt Low Power Design, Supply Voltage 3.3 VDC ( $\pm 5\%$ )
- Supply Current 350 mA typ. at 66 MHz
- Size 45 x 45 mm

## 2 PINOUTS

The 169 pins of the PGA socket are associated to 17 lines and 17 columns. The individual lines are allocated to digits; letters localize the columns.

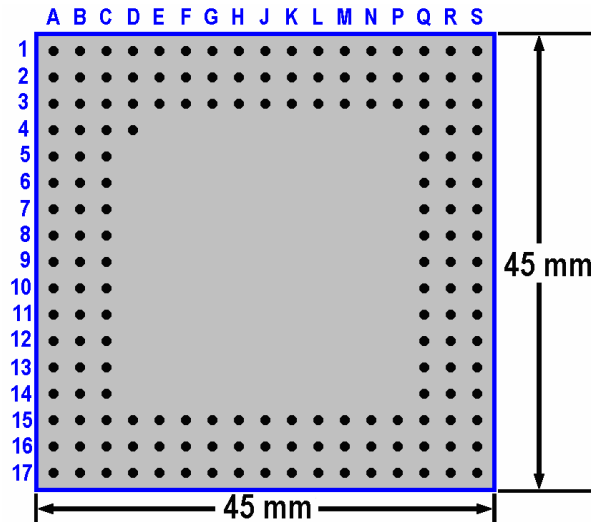


Figure 4: PNP/5280 pin side view

The following tables 1-17 show the pinout of the PNP/5280.

**Please note:** The notation of letters is not continuous. The letters „I“ and „O“ are not provided. These columns are not available.

### 2.1 PGA-169 Pins A1 – A17

| Pin | Name | Function   |
|-----|------|--|
| A1  | RX1- | Ethernet LAN1 Interface, RX-                       |
| A2  | TX1- | Ethernet LAN1 Interface, TX-                       |
| A3  | RX2- | Ethernet LAN2 Interface, RX-                       |
| A4  | TX2- | Ethernet LAN2 Interface, TX-                       |
| A5  | ---  | Reserved   |
| A6  | ---  | Reserved   |
| A7  | ---  | Reserved   |
| A8  | Fix0 | This Pin is always '0' (internal connected to GND) |
| A9  | SA22 | Expansion Bus, Address Bit 22                      |
| A10 | SA20 | Expansion Bus, Address Bit 20                      |
| A11 | SA18 | Expansion Bus, Address Bit 18                      |
| A12 | SA16 | Expansion Bus, Address Bit 16                      |
| A13 | SA13 | Expansion Bus, Address Bit 13                      |
| A14 | SA10 | Expansion Bus, Address Bit 10                      |
| A15 | SA8  | Expansion Bus, Address Bit 8                       |
| A16 | SA7  | Expansion Bus, Address Bit 7                       |
| A17 | SA6  | Expansion Bus, Address Bit 6                       |

Table 1: Pins A1 – A17

## 2.2 PGA-169 Pins B1 – B17

| Pin | Name | Function   |
|-----|------|--|
| B1  | RX1+ | Ethernet LAN1 Interface, RX+                       |
| B2  | TX1+ | Ethernet LAN1 Interface, TX+                       |
| B3  | RX2+ | Ethernet LAN2 Interface, RX+                       |
| B4  | TX2+ | Ethernet LAN2 Interface, TX+                       |
| B5  | ---  | Reserved   |
| B6  | ---  | Reserved   |
| B7  | Fix0 | This Pin is always '0' (internal connected to GND) |
| B8  | SA23 | Expansion Bus, Address Bit 23                      |
| B9  | SA21 | Expansion Bus, Address Bit 21                      |
| B10 | SA19 | Expansion Bus, Address Bit 19                      |
| B11 | SA17 | Expansion Bus, Address Bit 17                      |
| B12 | SA15 | Expansion Bus, Address Bit 15                      |
| B13 | SA12 | Expansion Bus, Address Bit 12                      |
| B14 | SA9  | Expansion Bus, Address Bit 9                       |
| B15 | SA5  | Expansion Bus, Address Bit 5                       |
| B16 | SA3  | Expansion Bus, Address Bit 3                       |
| B17 | SA4  | Expansion Bus, Address Bit 4                       |

Table 2: Pins B1 – B17

## 2.3 PGA-169 Pins C1 – C17

| Pin | Name | Function                                |
|-----|------|---|
| C1  | TXD1 | COM1 Serial Port, TXD Pin               |
| C2  | RXD1 | COM1 Serial Port, RXD Pin               |
| C3  | VBAT | Real Time Clock Battery Input           |
| C4  | GND  | Ground                                  |
| C5  | RCME | Remote Console Mode Enable (Low-active) |
| C6  | VCC  | 3.3 Volt Power Input                    |
| C7  | GND  | Ground                                  |
| C8  | GND  | Ground                                  |
| C9  | GND  | Ground                                  |
| C10 | GND  | Ground                                  |
| C11 | GND  | Ground                                  |
| C12 | VCC  | 3.3 Volt Power Input                    |
| C13 | SA14 | Expansion Bus, Address Bit 14           |
| C14 | SA11 | Expansion Bus, Address Bit 11           |
| C15 | SA2  | Expansion Bus, Address Bit 2            |
| C16 | SA0  | Expansion Bus, Address Bit 0            |
| C17 | SA1  | Expansion Bus, Address Bit 1            |

Table 3: Pins C1 – C17

## 2.4 PGA-169 Pins D1 – D17

| Pin | Name | Function                          |
|-----|------|-----------------------------------|
| D1  | TXD2 | COM2 Serial Port, TXD Pin         |
| D2  | RXD2 | COM2 Serial Port, RXD Pin         |
| D3  | GND  | Ground                            |
| D4  | GND  | Ground                            |
|     |      |                                   |
| D15 | CS3  | Chip Select Output 3 (Low-active) |
| D16 | CS1  | Chip Select Output 1 (Low-active) |
| D17 | CS2  | Chip Select Output 2 (Low-active) |

Table 4: Pins D1 – D17

## 2.5 PGA-169 Pins E1 – E17

| Pin | Name     | Function                             |
|-----|----------|--------------------------------------|
| E1  | ERXD2    | MII Receive Data Bit 2               |
| E2  | ERXD3    | MII Receive Data Bit 3               |
| E3  | LAN1.LED | Activity LED Ethernet LAN1 Interface |
|     |          |                                      |
| E15 | RDY      | External Ready Input                 |
| E16 | CS4      | Chip Select Output 4 (Low-active)    |
| E17 | CS5      | Chip Select Output 5 (Low-active)    |

Table 5: Pins E1 – E17

## 2.6 PGA-169 Pins F1 – F17

| Pin | Name  | Function   |
|-----|-------|--|
| F1  | ERXD0 | MII Receive Data Bit 0                             |
| F2  | ERXD1 | MII Receive Data Bit 1                             |
| F3  | VCC   | 3.3 Volt Power Input                               |
|     |       |  |
| F15 | VCC   | 3.3 Volt Power Input                               |
| F16 | OE    | Expansion Bus, Output Enable (Output - Low-active) |
| F17 | WE    | Expansion Bus, Write Enable (Output - Low-active)  |

Table 6: Pins F1 – F17

## 2.7 PGA-169 Pins G1 – G17

| Pin | Name   | Function               |
|-----|--------|------------------------|
| G1  | ERXDV  | MII Receive Data Valid |
| G2  | ERXCLK | MII Receive Clock      |
| G3  | GND    | Ground                 |
|     |        |                        |
| G15 | GND    | Ground                 |
| G16 | ---    | Reserved               |
| G17 | ---    | Reserved               |

Table 7: Pins G1 – G17



## 2.8 PGA-169 Pins H1 – H17

| Pin | Name  | Function                  |
|-----|-------|---------------------------|
| H1  | EMDC  | MII Management Data Clock |
| H2  | ERXER | MII Receive Error         |
| H3  | GND   | Ground                    |
|     |       |                           |
| H15 | GND   | Ground                    |
| H16 | ---   | Reserved                  |
| H17 | ---   | Reserved                  |

Table 8: Pins H1 – H17

## 2.9 PGA-169 Pins J1 – J17

| Pin | Name | Function             |
|-----|------|----------------------|
| J1  | ECRS | MII Carrier Sense    |
| J2  | ECOL | MII Collision Detect |
| J3  | GND  | Ground               |
|     |      |                      |
| J15 | GND  | Ground               |
| J16 | ---  | Reserved             |
| J17 | ---  | Reserved             |

Table 9: Pins J1 – J17

## 2.10 PGA-169 Pins K1 – K17

| Pin | Name  | Function                |
|-----|-------|-------------------------|
| K1  | EMDIO | MII Management Data I/O |
| K2  | ETXER | MII Transmit Error      |
| K3  | GND   | Ground                  |
|     |       |                         |
| K15 | GND   | Ground                  |
| K16 | ---   | Reserved                |
| K17 | ---   | Reserved                |

Table 10: Pins K1 – K17

## 2.11 PGA-169 Pins L1 – L17

| Pin | Name   | Function            |
|-----|--------|---------------------|
| L1  | ETXEN  | MII Transmit Enable |
| L2  | ETXCLK | MII Transmit Clock  |
| L3  | GND    | Ground              |
|     |        |                     |
| L15 | GND    | Ground              |
| L16 | ---    | Reserved            |
| L17 | ---    | Reserved            |

Table 11: Pins L1 – L17

## 2.12 PGA-169 Pins M1 – M17

| Pin | Name  | Function   |
|-----|-------|--|
| M1  | ETXD0 | MII Transmit Data Bit 0                          |
| M2  | ETXD1 | MII Transmit Data Bit 1                          |
| M3  | VCC   | 3.3 Volt Power Input                             |
|     |       |  |
| M15 | VCC   | 3.3 Volt Power Input                             |
| M16 | RD/WR | Read/Write Signal (Output - Write is Low-active) |
| M17 | INT1  | Interrupt Input 1                                |

Table 12: Pins M1 – M17

## 2.13 PGA-169 Pins N1 – N17

| Pin | Name     | Function                             |
|-----|----------|--------------------------------------|
| N1  | ETXD2    | MII Transmit Data Bit 2              |
| N2  | ETXD3    | MII Transmit Data Bit 3              |
| N3  | LAN2.LED | Activity LED Ethernet LAN2 Interface |
|     |          |                                      |
| N15 | CLKOUT   | Clock Output                         |
| N16 | RESIN    | RESET Input (Low-active)             |
| N17 | RESOUT   | RESET Output (Low-active)            |

Table 13: Pins N1 – N17

## 2.14 PGA-169 Pins P1 – P17

| Pin | Name | Function                    |
|-----|------|-----------------------------|
| P1  | PC2  | Parallel I/O, Port C, Bit 2 |
| P2  | PC1  | Parallel I/O, Port C, Bit 1 |
| P3  | PC3  | Parallel I/O, Port C, Bit 3 |
|     |      |                             |
| P15 | SD2  | Expansion Bus, Data Bit 2   |
| P16 | SD0  | Expansion Bus, Data Bit 0   |
| P17 | SD1  | Expansion Bus, Data Bit 1   |

Table 14: Pins P1 – P17

## 2.15 PGA-169 Pins Q1 – Q17

| Pin | Name | Function                    |
|-----|------|-----------------------------|
| Q1  | PC0  | Parallel I/O, Port C, Bit 0 |
| Q2  | PB2  | Parallel I/O, Port B, Bit 2 |
| Q3  | PB5  | Parallel I/O, Port B, Bit 5 |
| Q4  | PA5  | Parallel I/O, Port A, Bit 5 |
| Q5  | PA2  | Parallel I/O, Port A, Bit 2 |
| Q6  | VCC  | 3.3 Volt Power Input        |
| Q7  | GND  | Ground                      |
| Q8  | GND  | Ground                      |
| Q9  | GND  | Ground                      |
| Q10 | GND  | Ground                      |
| Q11 | GND  | Ground                      |
| Q12 | VCC  | 3.3 Volt Power Input        |
| Q13 | SD17 | Expansion Bus, Data Bit 17  |
| Q14 | SD14 | Expansion Bus, Data Bit 14  |
| Q15 | SD5  | Expansion Bus, Data Bit 5   |
| Q16 | SD3  | Expansion Bus, Data Bit 3   |
| Q17 | SD4  | Expansion Bus, Data Bit 4   |

Table 15: Pins Q1 – Q17

## 2.16 PGA-169 Pins R1 – R17

| Pin | Name | Function                    |
|-----|------|-----------------------------|
| R1  | PB0  | Parallel I/O, Port B, Bit 0 |
| R2  | PB4  | Parallel I/O, Port B, Bit 4 |
| R3  | PB7  | Parallel I/O, Port B, Bit 7 |
| R4  | PA3  | Parallel I/O, Port A, Bit 3 |
| R5  | PA0  | Parallel I/O, Port A, Bit 0 |
| R6  | SD30 | Expansion Bus, Data Bit 30  |
| R7  | SD28 | Expansion Bus, Data Bit 28  |
| R8  | SD26 | Expansion Bus, Data Bit 26  |
| R9  | SD24 | Expansion Bus, Data Bit 24  |
| R10 | SD22 | Expansion Bus, Data Bit 22  |
| R11 | SD20 | Expansion Bus, Data Bit 20  |
| R12 | SD18 | Expansion Bus, Data Bit 18  |
| R13 | SD15 | Expansion Bus, Data Bit 15  |
| R14 | SD12 | Expansion Bus, Data Bit 12  |
| R15 | SD8  | Expansion Bus, Data Bit 8   |
| R16 | SD6  | Expansion Bus, Data Bit 6   |
| R17 | SD7  | Expansion Bus, Data Bit 7   |

Table 16: Pins R1 – R17

## 2.17 PGA-169 Pins S1 – S17

| Pin | Name | Function                    |
|-----|------|-----------------------------|
| S1  | PB1  | Parallel I/O, Port B, Bit 1 |
| S2  | PB3  | Parallel I/O, Port B, Bit 3 |
| S3  | PB6  | Parallel I/O, Port B, Bit 6 |
| S4  | PA4  | Parallel I/O, Port A, Bit 4 |
| S5  | PA1  | Parallel I/O, Port A, Bit 1 |
| S6  | SD31 | Expansion Bus, Data Bit 31  |
| S7  | SD29 | Expansion Bus, Data Bit 29  |
| S8  | SD27 | Expansion Bus, Data Bit 27  |
| S9  | SD25 | Expansion Bus, Data Bit 25  |
| S10 | SD23 | Expansion Bus, Data Bit 23  |
| S11 | SD21 | Expansion Bus, Data Bit 21  |
| S12 | SD19 | Expansion Bus, Data Bit 19  |
| S13 | SD16 | Expansion Bus, Data Bit 16  |
| S14 | SD13 | Expansion Bus, Data Bit 13  |
| S15 | SD11 | Expansion Bus, Data Bit 11  |
| S16 | SD10 | Expansion Bus, Data Bit 10  |
| S17 | SD9  | Expansion Bus, Data Bit 9   |

**Table 17: Pins S1 – S17**

### 3 PIO SIGNALS

Some PIO pins at the DIL/NetPC PNP/5280 PGA-169 connector are multifunction pins with a primary function and a secondary function. The default use is identical to the primary function.

| Pin | Name | Primary Function            | Secondary Function |
|-----|------|-----------------------------|--------------------|
| R5  | PA0  | Parallel I/O, Port A, Bit 0 | ---                |
| S5  | PA1  | Parallel I/O, Port A, Bit 1 | ---                |
| Q5  | PA2  | Parallel I/O, Port A, Bit 2 | ---                |
| R4  | PA3  | Parallel I/O, Port A, Bit 3 | ---                |
| S4  | PA4  | Parallel I/O, Port A, Bit 4 | ---                |
| Q4  | PA5  | Parallel I/O, Port A, Bit 5 | ---                |
| R1  | PB0  | Parallel I/O, Port B, Bit 0 | ---                |
| S1  | PB1  | Parallel I/O, Port B, Bit 1 | ---                |
| Q2  | PB2  | Parallel I/O, Port B, Bit 2 | ---                |
| S2  | PB3  | Parallel I/O, Port B, Bit 3 | ---                |
| R2  | PB4  | Parallel I/O, Port B, Bit 4 | SCL (I2C)          |
| Q3  | PB5  | Parallel I/O, Port B, Bit 5 | SDA (I2C)          |
| S3  | PB6  | Parallel I/O, Port B, Bit 6 | CANTX (CAN)        |
| R3  | PB7  | Parallel I/O, Port B, Bit 7 | CANRX (CAN)        |
| Q1  | PC0  | Parallel I/O, Port C, Bit 0 | QSPIDO (SPI)       |
| P2  | PC1  | Parallel I/O, Port C, Bit 1 | QSPIDI (SPI)       |
| P1  | PC2  | Parallel I/O, Port C, Bit 2 | QSPICLK (SPI)      |
| P3  | PC3  | Parallel I/O, Port C, Bit 3 | QSPICS0 (SPI)      |

**Table 18: PIO signals of the PNP/5280 PGA-169 connector**

## 4 LAN SIGNALS

The three different LAN configurations of the PNP/5280 offers three different pin outs for the 10/100 Mbps Ethernet LAN interface.

Table 19 shows the PGA-169 connector usage of the PNP/5280-M, the PNP/5280 version with MII (Media Independent Interface) for external PHY or switch devices.

| Pin | Name   | Function                  |
|-----|--------|---------------------------|
| J2  | ECOL   | MII Collision Detect      |
| J1  | ECRS   | MII Carrier Sense         |
| H1  | EMDC   | MII Management Data Clock |
| K1  | EMDIO  | MII Management Data I/O   |
| G2  | ERXCLK | MII Receive Clock         |
| F1  | ERXD0  | MII Receive Data Bit 0    |
| F2  | ERXD1  | MII Receive Data Bit 1    |
| E1  | ERXD2  | MII Receive Data Bit 2    |
| E2  | ERXD3  | MII Receive Data Bit 3    |
| G1  | ERXDV  | MII Receive Data Valid    |
| H2  | ERXER  | MII Receive Error         |
| L2  | ETXCLK | MII Transmit Clock        |
| M1  | ETXD0  | MII Transmit Data Bit 0   |
| M2  | ETXD1  | MII Transmit Data Bit 1   |
| N1  | ETXD2  | MII Transmit Data Bit 2   |
| N2  | ETXD3  | MII Transmit Data Bit 3   |
| L1  | ETXEN  | MII Transmit Enable       |
| K2  | ETXER  | MII Transmit Error        |

**Table 19: PNP/5280-M LAN Signals**

Table 20 shows the PGA-169 connector usage of the PNP/5280-N, the PNP/5280 version with an on-board PHY device.

**Please note:** Do not use the MII signals from table 19 with a PNP/5280-N. Leave this pins unconnected in your PNP/5280-based design.

| Pin | Name | Function                     |
|-----|------|------------------------------|
| A1  | RX1- | Ethernet LAN1 Interface, RX- |
| A2  | TX1- | Ethernet LAN1 Interface, TX- |
| B1  | RX1+ | Ethernet LAN1 Interface, RX+ |
| B2  | TX1+ | Ethernet LAN1 Interface, TX+ |

**Table 20: PNP/5280-N LAN Signals**

Table 21 shows the PGA-169 connector usage of the PNP/5280-S, the PNP/5280 version with an on-board 3-port integrated switch chip.

**Please note:** Do not use the MII signals from table 19 with a PNP/5280-S. Leave this pins unconnected in your PNP/5280-based design.

| Pin | Name | Function                     |
|-----|------|------------------------------|
| A1  | RX1- | Ethernet LAN1 Interface, RX- |
| A2  | TX1- | Ethernet LAN1 Interface, TX- |
| A3  | RX2- | Ethernet LAN2 Interface, RX- |
| A4  | TX2- | Ethernet LAN2 Interface, TX- |
| B1  | RX1+ | Ethernet LAN1 Interface, RX+ |
| B2  | TX1+ | Ethernet LAN1 Interface, TX+ |
| B3  | RX2+ | Ethernet LAN2 Interface, RX+ |
| B4  | TX2+ | Ethernet LAN1 Interface, TX+ |

**Table 21: PNP/5280-S LAN Signals**

## 5 MECHANICAL DIMENSIONS

The PNP/5280 uses a 169-pin PGA socket format (SOCKET 3) as a mechanical base. The following figure shows the dimensions. All length dimensions have a tolerance of 0.5 mm. All other 0.1 mm.

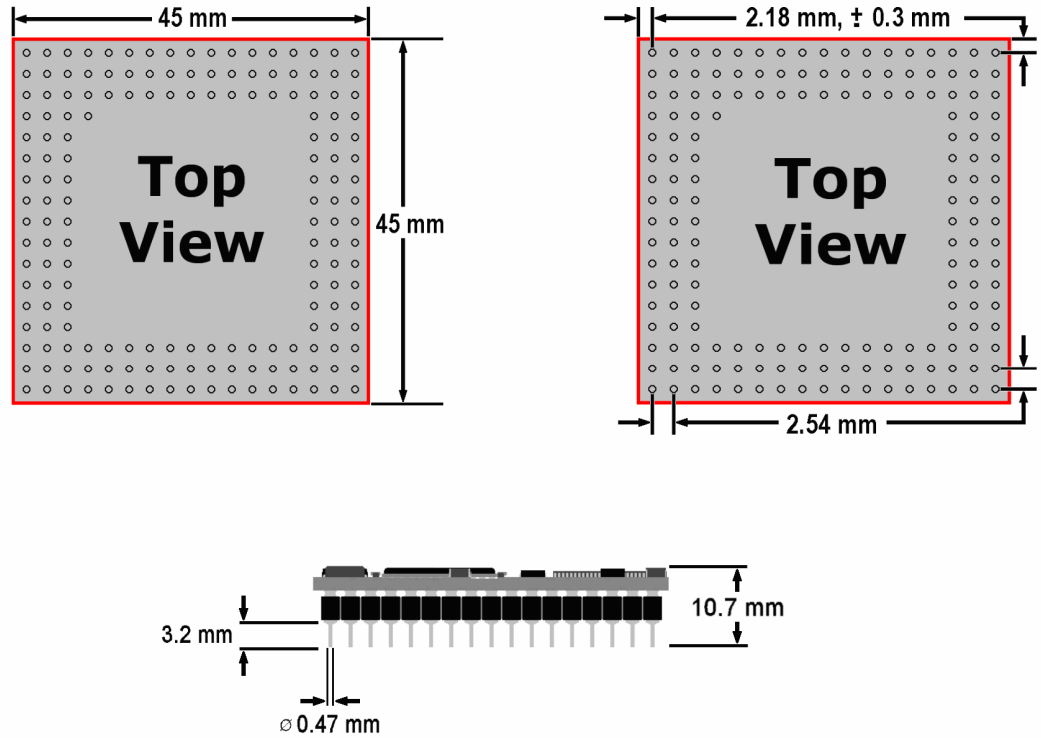


Figure 5: Mechanical dimensions of PNP/5280



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## DOCUMENT HISTORY

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| Revision | Date       | Remarks       | Name |
|----------|------------|---------------|------|
| 1.0      | 2005-05-03 | first version | WBU  |

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