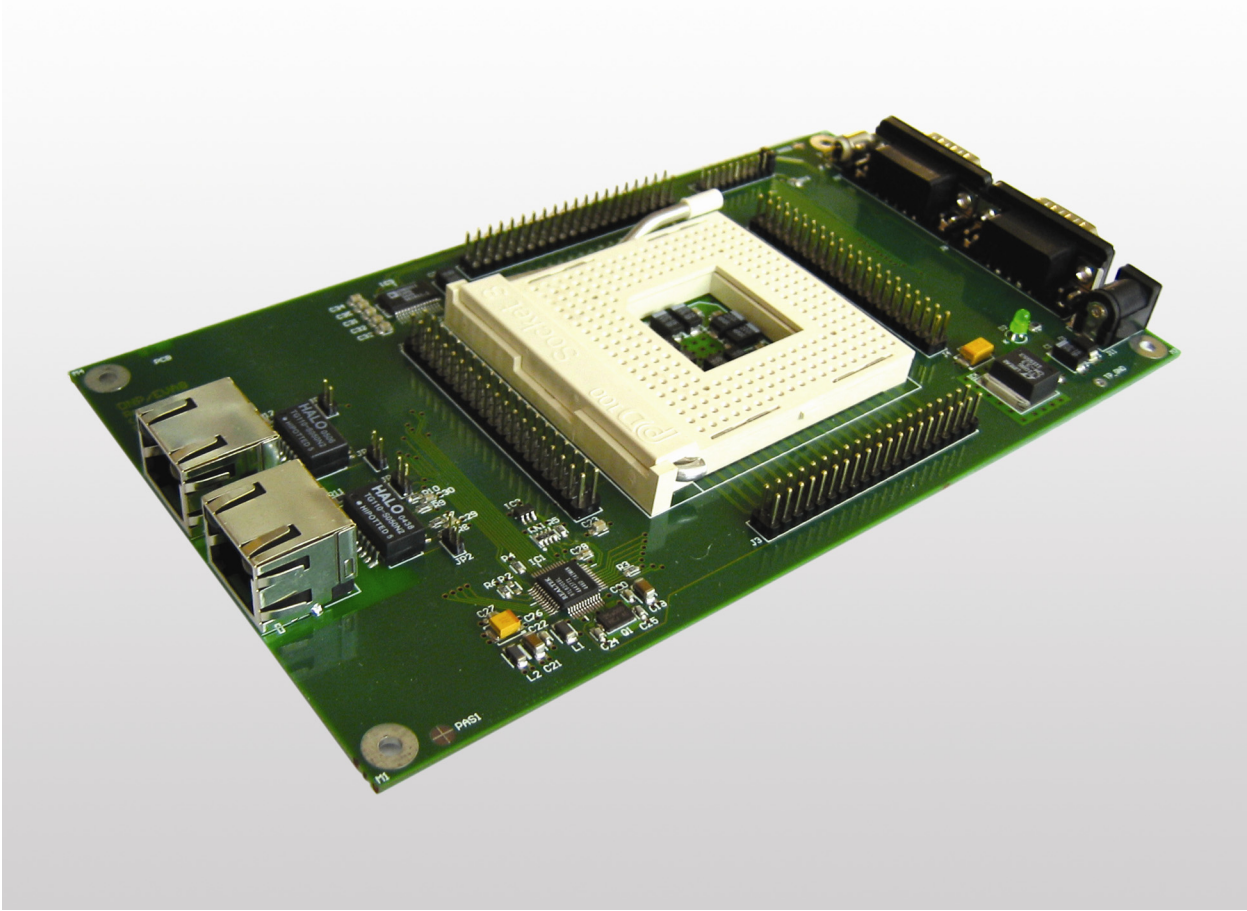
DNP/EVA8

Board Revision 1.0

Hardware Reference



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Manual Revision: 1.0
Date: 2005-05-03

For further information regarding our products please visit us at www.dilnetpc.com

CONTENT

1 INTRODUCTION

This document describes the hardware components of the DNP/EVA8. The DNP/EVA8 is an evaluation board for the DIL/NetPC PNP/5280. For further information about the individual components of this product you may follow the links from our website at http://www.dilnetpc.com. Our website contains a lot of technical information, which will be updated in regular periods.

The PNP/5280 is available in three different 10/100 Mbps Ethernet LAN configurations. The version with the order code **PNP/5280-M** offers the 10/100 Ethernet MII (Media Independent Interface) signals on the 169-pin PGA connector. With the order code **PNP/5280-N** comes a PNP/5280 version with an on-board PHY chip and one 10/100 Ethernet LAN interface. The order code **PNP/5280-S** is assigned to a PNP/5280 version with an on-board 3-port integrated switch chip with two embedded PHY devices. The PNP/5280-S offers two 10/100 Ethernet LAN interfaces.

There are three different version of the DNP/EVA8 evaluation board available. The version with the order code **DNP/EVA8-M** supports the PNP/5280-M. The **DNP/EVA8-N** offers the LAN environment for the PNP/5280-N. The **DNP/EVA8-S** supports the PNP/5280-S with two LAN interfaces.

1.1 Block Diagram DNP/EVA8-M

Figure 1 shows the block diagram of the DNP/EVA8-M. This version of the evaluation board supports the PNP/5280-M with MII interface. The DNP/EVA8-M comes with a on-board 10/100 Mbps PHY chip, the necessary LAN magnetics and one RJ45 connector for standard 10/100 Mbps Ethernet LAN cables. The PHY chip (Realtek RTL8201 or similar) is connected to the PNP/5280 MII signals.

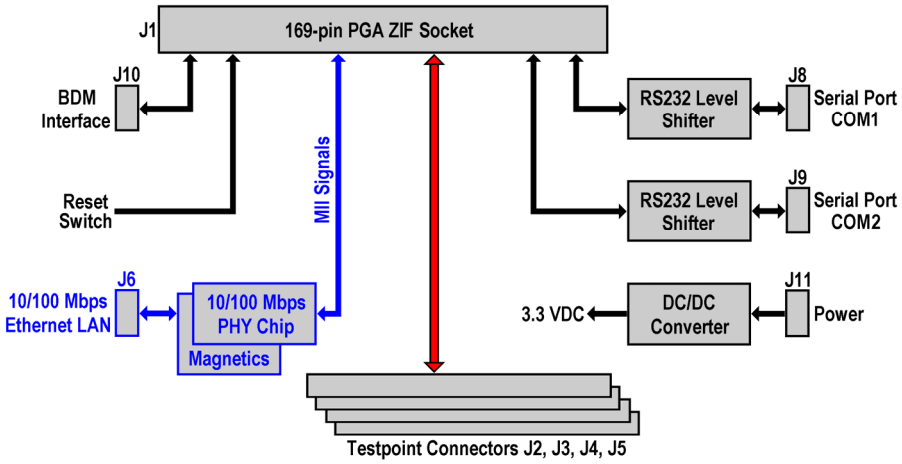


Figure 1: Block diagram of DNP/EVA8-M for PNP/5280-M

1.2 Block Diagram DNP/EVA8-N

Figure 2 shows the block diagram of the DNP/EVA8-N. This version of the evaluation board supports the PNP/5280-N with one 10/100 Mbps Ethernet LAN interface. The DNP/EVA8-N includes the necessary LAN magnetics and one RJ45 connector for standard 10/100 Mbps Ethernet LAN cables. The LAN magnetics is connected to the PNP/5280 LAN1 signals.

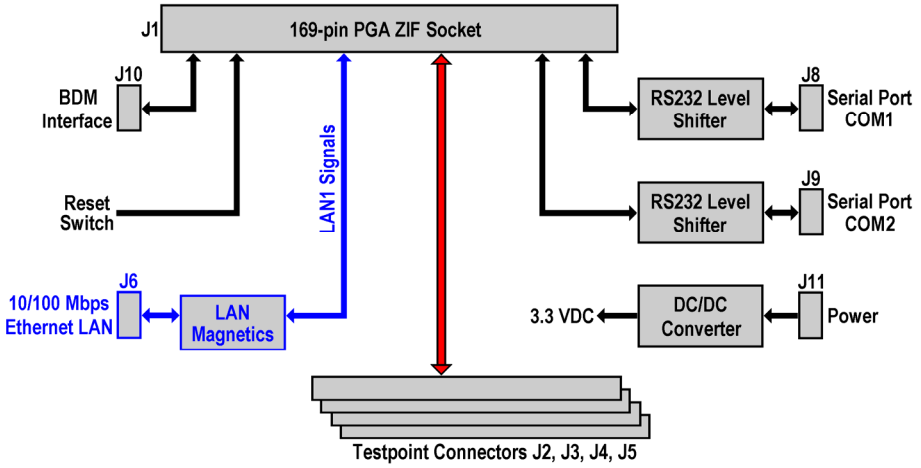


Figure 2: Block diagram of DNP/EVA8-N for PNP/5280-N

1.3 Block Diagram DNP/EVA8-S

Figure 3 shows the block diagram of the DNP/EVA8-S. This version of the evaluation board supports the PNP/5280-S with two 10/100 Mbps Ethernet LAN interface. The DNP/EVA8-S includes the necessary LAN magnetics and two RJ45 connectors for standard 10/100 Mbps Ethernet LAN cables. The LAN magnetics are connected to the PNP/5280 LAN1 and LAN2 signals.

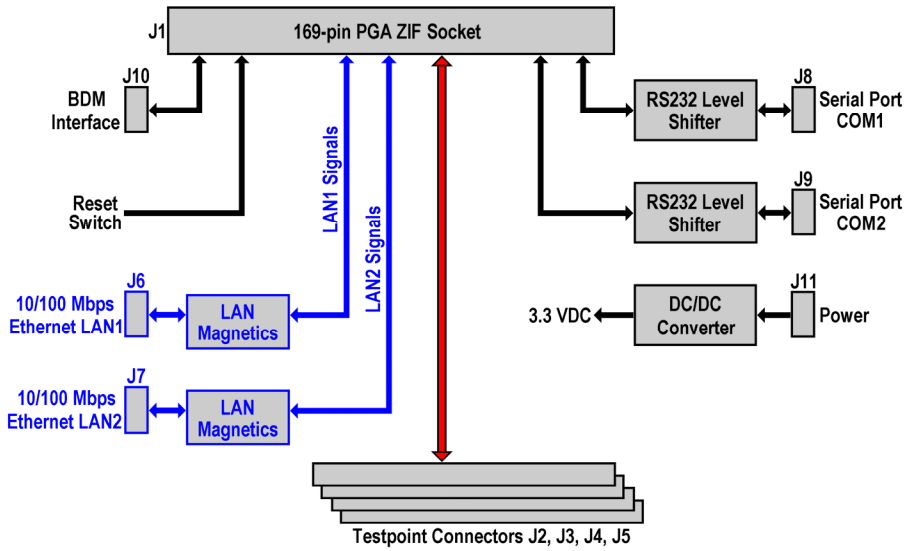


Figure 3: Block diagram of DNP/EVA8-S for PNP/5280-S

1.4 Features DNP/EVA8

- One 169-pin PGA ZIF (Zero Insertion Force) Socket
- Two RS232 Interfaces with Level Shifter and Sub-D Connectors
- External Reset Switch for manual Reset
- 3.3 V DC/DC Converter
- One Power LED
- BDM Interface Connector
- DNP/EVA8-M: On-board PHY chip, one RJ45 and one LAN Magnetics for MII usage of PNP/5280-M
- DNP/EVA8-N: One RJ45 and LAN Magnetics for LAN1 usage of PNP/5280-N
- DNP/EVA8-S: Two RJ45 and LAN Magnetics for LAN1/LAN2 usage of PNP/5280-S
- Supply Voltage 3.3 VDC
- Board Dimension 180 x 100 mm

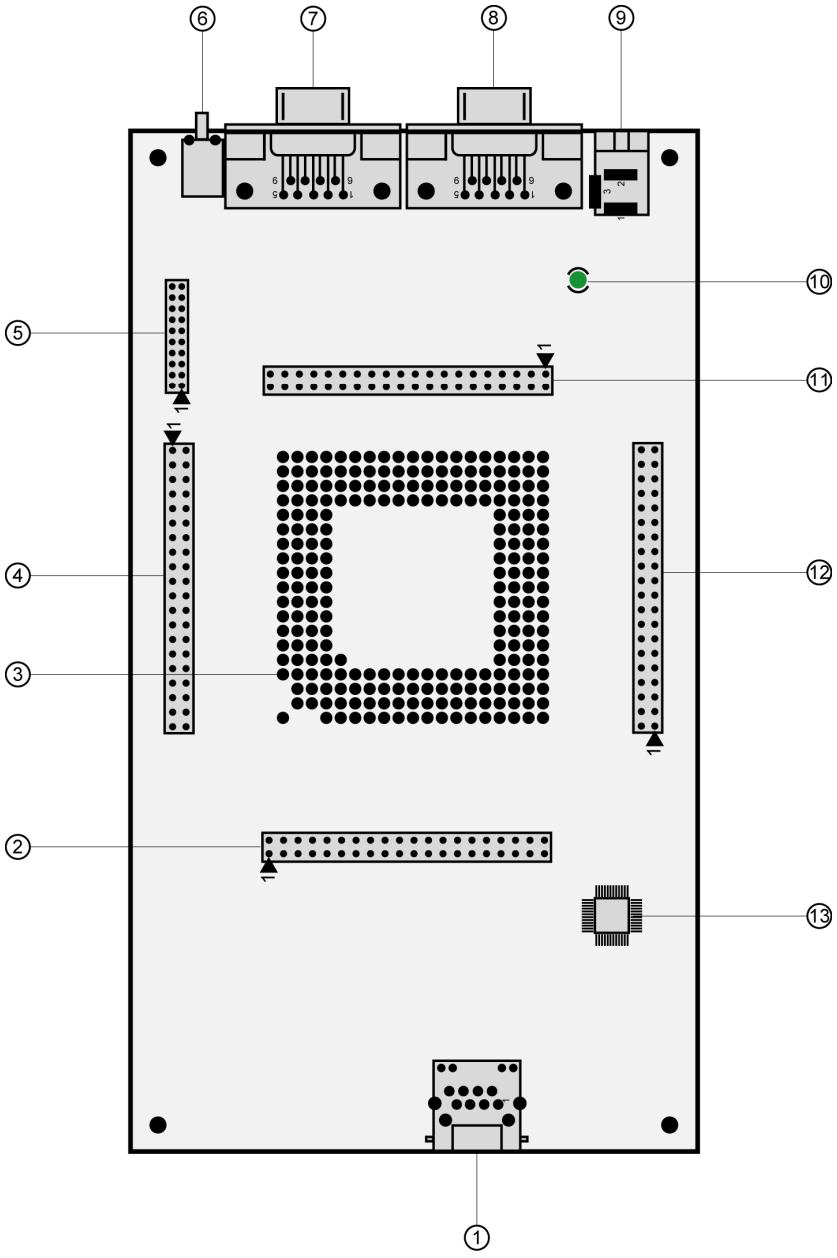
Order Code	LAN Interfaces	On-board PHY chip	Jumper JP1-JP4
DNP/EVA8-M	1 x 10/100 Mbps	Yes (1 x Realtek RTL8201)	Open
DNP/EVA8-N	1 x 10/100 Mbps	No	Open
DNP/EVA8-S	2 x 10/100 Mbps	No	Closed

Table 1: DNP/EVA8 order codes and configurations

The Jumpers JP1 – JP4 are factory setup options. Please do not change these jumpers on your DNP/EVA8 evaluation board.

2 BOARD LAYOUT

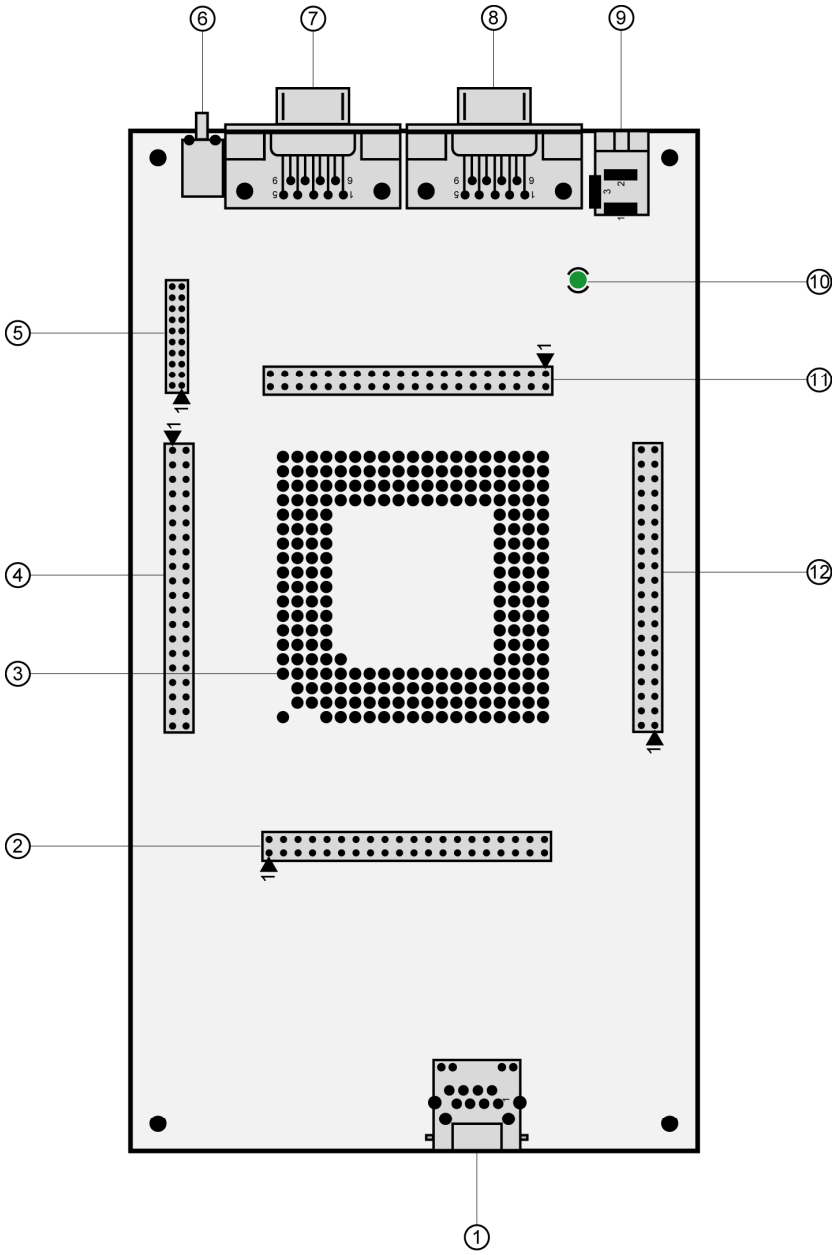
2.1 Board Layout DNP/EVA8-M



① J6 - 10/100 Mbps Ethernet LAN1
② J2 - Testpoint connector
③ J1 - ZIF socket
④ J5 - Testpoint connector
⑤ J10 - BDM interface
⑥ S1 - Reset button
⑦ J9 - Serial port COM2
⑧ J8 - Serial port COM1
⑨ J11 - Power connector
⑩ D2 - Power LED
⑪ J4 - Testpoint connector
⑫ J3 - Testpoint connector
⑬ IC1 - Ethernet PHY chip

Figure 4: Top view DNP/EVA8-M

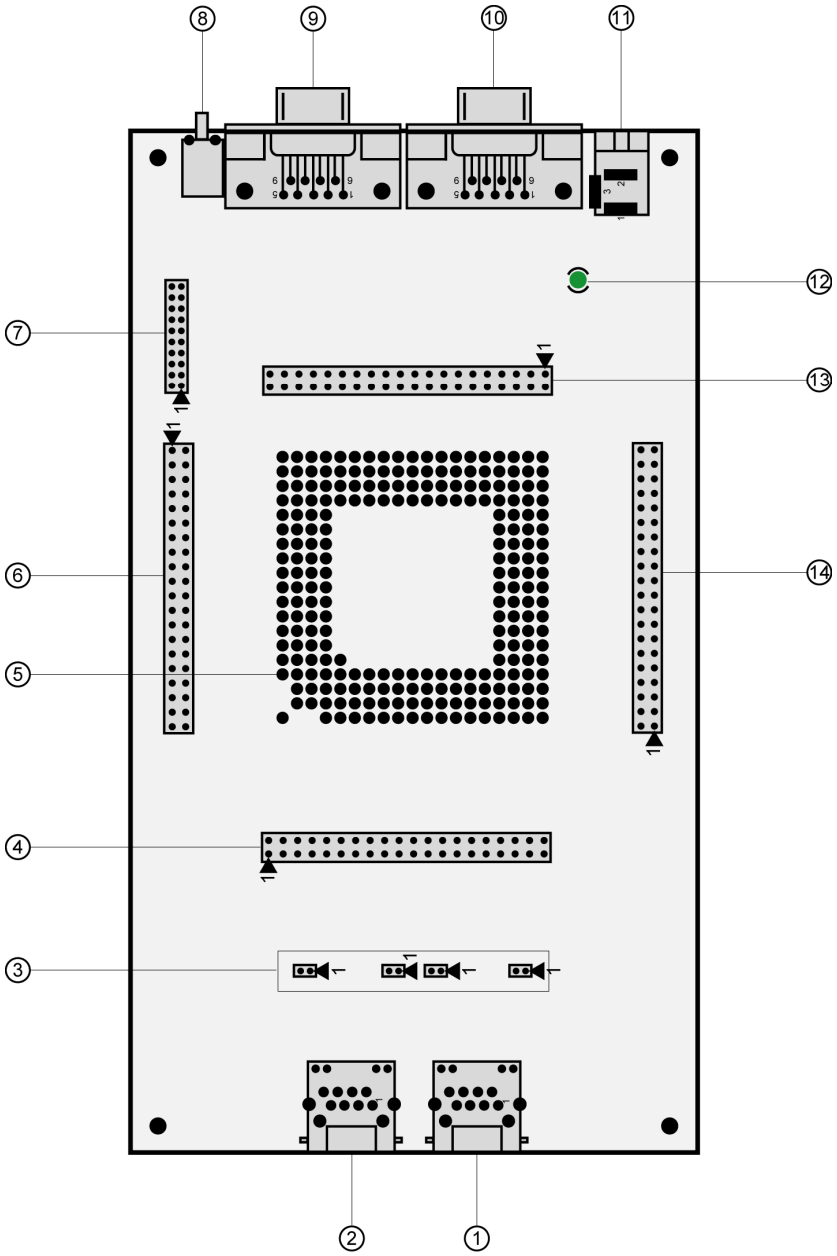
2.2 Board Layout DNP/EVA8-N



① J6 - 10/100 Mbps Ethernet LAN1
② J2 - Testpoint connector
③ J1 - ZIF socket
④ J5 - Testpoint connector
⑤ J10 - BDM interface
⑥ S1 - Reset button
⑦ J9 - Serial port COM2
⑧ J8 - Serial port COM1
⑨ J11 - Power connector
⑩ D2 - Power LED
⑪ J4 - Testpoint connector
⑫ J3 - Testpoint connector

Figure 5: Top view DNP/EVA8-N

2.3 Board Layout DNP/EVA8-S



① J6 - 10/100 Mbps Ethernet LAN1
② J7 - 10/100 Mbps Ethernet LAN2
③ JP1 to JP4 - LAN jumper
④ J2 - Testpoint connector
⑤ J1 - ZIF socket
⑥ J5 - Testpoint connector
⑦ J10 - BDM interface
⑧ S1 - Reset button
⑨ J9 - Serial port COM2
⑩ J8 - Serial port COM1
⑪ J11 - Power connector
⑫ D2 - Power LED
⑬ J4 - Testpoint connector
⑭ J3 - Testpoint connector

Figure 6: Top view DNP/EVA8-S

3 PINOUTS

3.1 Testpoint Connector – J2 (Mapping to PGA169 – J1)

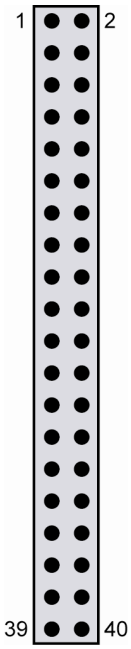
Top View	Pin	Name	Function
	1	VCC3	Power
	2	GND	Ground
	3	---	Not Connected
	4	---	Not Connected
	5	A2	Ethernet LAN1 Interface, TX-
	6	A1	Ethernet LAN1 Interface, RX-
	7	B2	Ethernet LAN1 Interface, TX+
	8	B1	Ethernet LAN1 Interface, RX+
	9	C2	COM1 Serial Port, RXD Pin
	10	C1	COM1 Serial Port, TXD Pin
	11	D2	COM2 Serial Port, RXD Pin
	12	D1	COM2 Serial Port, TXD Pin
	13	E2	MII Receive Data Bit 3
	14	E1	MII Receive Data Bit 2
	15	F2	MII Receive Data Bit 1
	16	F1	MII Receive Data Bit 0
	17	G2	MII Receive Clock
	18	G1	MII Receive Data Valid
	19	H2	MII Receive Error
	20	H1	MII Management Data Clock
	21	J2	MII Collision Detect
	22	J1	MII Carrier Sense
	23	K2	MII Transmit Error
	24	K1	MII Management Data I/O
	25	L2	MII Transmit Clock
	26	L1	MII Transmit Enable
	27	M2	MII Transmit Data Bit 1
	28	M1	MII Transmit Data Bit 0
	29	N2	MII Transmit Data Bit 3
	30	N1	MII Transmit Data Bit 2
	31	P2	Parallel I/O, Port C, Bit 1
	32	P1	Parallel I/O, Port C, Bit 2
	33	P3	Parallel I/O, Port C, Bit 3
	34	Q1	Parallel I/O, Port C, Bit 0
	35	---	Not Connected
	36	---	Not Connected
	37	---	Not Connected
	38	---	Not Connected
	39	---	Not Connected
	40	---	Not Connected

Table 2: Pinout J2

3.2 Testpoint Connector – J3 (Mapping to PGA169 – J1)

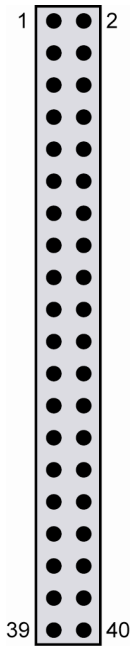
Top View	Pin	Name	Function
	1	VCC3	Power
	2	GND	Ground
	3	R1	Parallel I/O, Port B, Bit 0
	4	Q2	Parallel I/O, Port B, Bit 2
	5	S1	Parallel I/O, Port B, Bit 1
	6	R2	Parallel I/O, Port B, Bit 4
	7	Q3	Parallel I/O, Port B, Bit 5
	8	S2	Parallel I/O, Port B, Bit 3
	9	R3	Parallel I/O, Port B, Bit 7
	10	S3	Parallel I/O, Port B, Bit 6
	11	Q4	Parallel I/O, Port A, Bit 5
	12	R4	Parallel I/O, Port A, Bit 3
	13	S4	Parallel I/O, Port A, Bit 4
	14	Q5	Parallel I/O, Port A, Bit 2
	15	S5	Parallel I/O, Port A, Bit 1
	16	R5	Parallel I/O, Port A, Bit 0
	17	S6	Expansion Bus, Data Bit 31
	18	R6	Expansion Bus, Data Bit 30
	19	S7	Expansion Bus, Data Bit 29
	20	R7	Expansion Bus, Data Bit 28
	21	S8	Expansion Bus, Data Bit 27
	22	R8	Expansion Bus, Data Bit 26
	23	S9	Expansion Bus, Data Bit 25
	24	R9	Expansion Bus, Data Bit 24
	25	S10	Expansion Bus, Data Bit 23
	26	R10	Expansion Bus, Data Bit 22
	27	S11	Expansion Bus, Data Bit 21
	28	R11	Expansion Bus, Data Bit 20
	29	S12	Expansion Bus, Data Bit 19
	30	R12	Expansion Bus, Data Bit 18
	31	S13	Expansion Bus, Data Bit 16
	32	R13	Expansion Bus, Data Bit 15
	33	S14	Expansion Bus, Data Bit 13
	34	Q13	Expansion Bus, Data Bit 17
	35	S15	Expansion Bus, Data Bit 11
	36	R14	Expansion Bus, Data Bit 12
	37	S16	Expansion Bus, Data Bit 10
	38	Q14	Expansion Bus, Data Bit 14
	39	S17	Expansion Bus, Data Bit 9
	40	R15	Expansion Bus, Data Bit 8

Table 3: Pinout J3

3.3 Testpoint Connector – J4 (Mapping to PGA169 – J1)

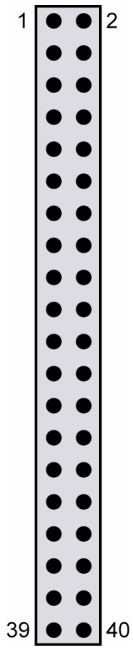
Top View	Pin	Name	Function
	1	VCC3	Power
	2	GND	Ground
	3	---	Not Connected
	4	---	Not Connected
	5	R16	Expansion Bus, Data Bit 6
	6	R17	Expansion Bus, Data Bit 7
	7	Q15	Expansion Bus, Data Bit 5
	8	Q16	Expansion Bus, Data Bit 3
	9	Q17	Expansion Bus, Data Bit 4
	10	P15	Expansion Bus, Data Bit 2
	11	P17	Expansion Bus, Data Bit 1
	12	P16	Expansion Bus, Data Bit 0
	13	---	Not Connected
	14	N15	Clock Output
	15	N17	RESET Output (Low-active)
	16	N16	RESET Input (Low-active)
	17	M17	Interrupt Input 1
	18	M16	Read/Write (Output – Write is Low-active)
	19	L17	Reserved
	20	L16	Reserved
	21	K17	Reserved
	22	K16	Reserved
	23	J17	Reserved
	24	J16	Reserved
	25	H17	Reserved
	26	H16	Reserved
	27	G17	Reserved
	28	G16	Reserved
	29	F17	Expansion Bus, Write Enable (Output – Low-active)
	30	F16	Expansion Bus, Output Enable (Output – Low-active)
	31	E15	External Ready Input
	32	---	Not Connected
	33	E17	Chip Select Output 5 (Low-active)
	34	E16	Chip Select Output 4 (Low-active)
	35	D17	Chip Select Output 2 (Low-active)
	36	D16	Chip Select Output 1 (Low-active)
	37	D15	Chip Select Output 3 (Low-active)
	38	C17	Expansion Bus, Address Bit 1
	39	C16	Expansion Bus, Address Bit 0
	40	C15	Expansion Bus, Address Bit 2

Table 4: Pinout J4

3.4 Testpoint Connector – J5 (Mapping to PGA169 – J1)

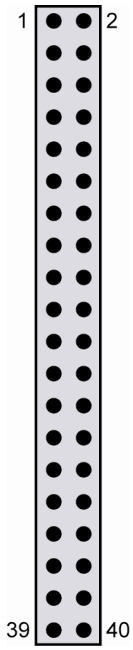
Top View	Pin	Name	Function
	1	VCC3	Power
	2	GND	Ground
	3	B17	Expansion Bus, Address Bit 4
	4	A17	Expansion Bus, Address Bit 6
	5	B16	Expansion Bus, Address Bit 3
	6	A16	Expansion Bus, Address Bit 7
	7	B15	Expansion Bus, Address Bit 5
	8	A15	Expansion Bus, Address Bit 8
	9	C14	Expansion Bus, Address Bit 11
	10	B14	Expansion Bus, Address Bit 9
	11	A14	Expansion Bus, Address Bit 10
	12	C13	Expansion Bus, Address Bit 14
	13	B13	Expansion Bus, Address Bit 12
	14	A13	Expansion Bus, Address Bit 13
	15	B12	Expansion Bus, Address Bit 15
	16	A12	Expansion Bus, Address Bit 16
	17	B11	Expansion Bus, Address Bit 17
	18	A11	Expansion Bus, Address Bit 18
	19	B10	Expansion Bus, Address Bit 19
	20	A10	Expansion Bus, Address Bit 20
	21	B9	Expansion Bus, Address Bit 21
	22	A9	Expansion Bus, Address Bit 22
	23	B8	Expansion Bus, Address Bit 23
	24	A8	This Pin is always ‘0’ (internal connected to GND)
	25	B7	This Pin is always ‘0’ (internal connected to GND)
	26	A7	Reserved
	27	B6	Reserved
	28	A6	Reserved
	29	B5	Reserved
	30	A5	Reserved
	31	C5	Remote Console Mode Enable (Low-active)
	32	C3	Real Time Clock Battery Input
	33	A4	Ethernet LAN2 Interface, TX-
	34	B4	Ethernet LAN2 Interface, TX+
	35	A3	Ethernet LAN2 Interface, RX-
	36	B3	Ethernet LAN2 Interface, RX+
	37	---	Not Connected
	38	---	Not Connected
	39	---	Not Connected
	40	---	Not Connected

Table 5: Pinout J5

3.5 10/100 Mbps Ethernet Interface (LAN1 and LAN2) – J6 and J7

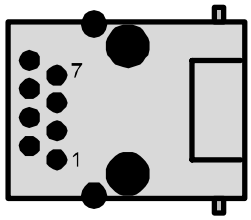
Top View	Pin	Name	Function
	1	TX+	10/100 Mbps LAN, TX+ pin
	2	TX-	10/100 Mbps LAN, TX- pin
	3	RX+	10/100 Mbps LAN, RX+ pin
	4	---	Not connected
	5	---	Not connected
	6	RX-	10/100 Mbps LAN, RX- pin
	7	---	Not connected
	8	---	Not connected

Table 6: Pinout 10/100 Mbps Ethernet interface

Note: J7 is only available on the DNP/EVA8-S.

3.6 RS232 Connector (Serial Port COM1) – J8

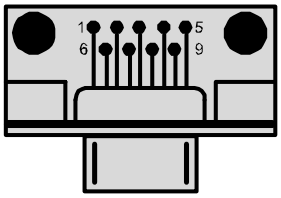
Top View	Pin	Name	Function
	1	DCD1	COM1 serial port, DCD pin
	2	RXD1	COM1 serial port, RXD pin
	3	TXD1	COM1 serial port, TXD pin
	4	DTR1	COM1 serial port, DTR pin
	5	GND1	Ground
	6	DSR1	COM1 serial port, DSR pin
	7	RTS1	COM1 serial port, RTS pin
	8	CTS1	COM1 serial port, CTS pin
	9	RI1	COM1 serial port, RI pin

Table 7: Pinout RS232 connector (COM1)

Note: All COM1 port signals are on RS232 level. There is no TTL level available on COM1.

3.7 RS232 Connector (Serial Port COM2) – J9

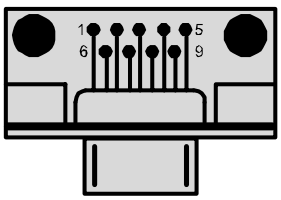
Top View	Pin	Name	Function
	1	DCD2	COM2 serial port, DCD pin
	2	RXD2	COM2 serial port, RXD pin
	3	TXD2	COM2 serial port, TXD pin
	4	DTR2	COM2 serial port, DTR pin
	5	GND2	Ground
	6	DSR2	COM2 serial port, DSR pin
	7	RTS2	COM2 serial port, RTS pin
	8	CTS2	COM2 serial port, CTS pin
	9	RI2	COM2 serial port, RI pin

Table 8: Pinout RS232 connector (COM2)

Note: All COM2 port signals are on RS232 level. There is no TTL level available on COM2.

3.8 BDM Interface – J10

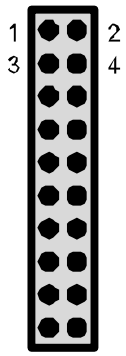
Top View	Pin	Name	Function
	1	VIO (3.3 VDC I/O Voltage)	Power
	2	GND	Ground
	3	TA#	BDM Function
	4	BKPT#	BDM Function
	5	Reset#	BDM Function
	6	DSCLK#	BDM Function
	7	DSI#	BDM Function
	8	TCLK	BDM Function
	9	PST3	BDM Function
	10	DS0	BDM Function
	11	PST2	BDM Function
	12	DDATA3	BDM Function
	13	PST1	BDM Function
	14	DDATA2	BDM Function
	15	PST0	BDM Function
	16	DDATA1	BDM Function
	17	PSTCLK	BDM Function
	18	DDATA0	BDM Function
	19	GND	Ground
	20	RCM	GPTB3

Table 9: DNP/EVA8 BDM interface

RCM Jumper (Pin 19 and 20)	Effects
Jumper not set	GPTB3 = 1 (High)
Jumper set	GPTB3 = 0 (Low)

Table 10: DNP/EVA8 RCM jumper

3.9 Power Connector – J11

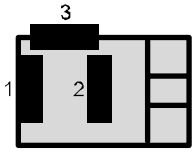
Top View	Pin	Name	Function
	1	Vcc	Power In
	2	GND	Ground
	3	GND	Ground

Table 11: Pinout power connector

4 MECHANICAL DIMENSIONS

All length dimensions have a tolerance of 0.5 mm.

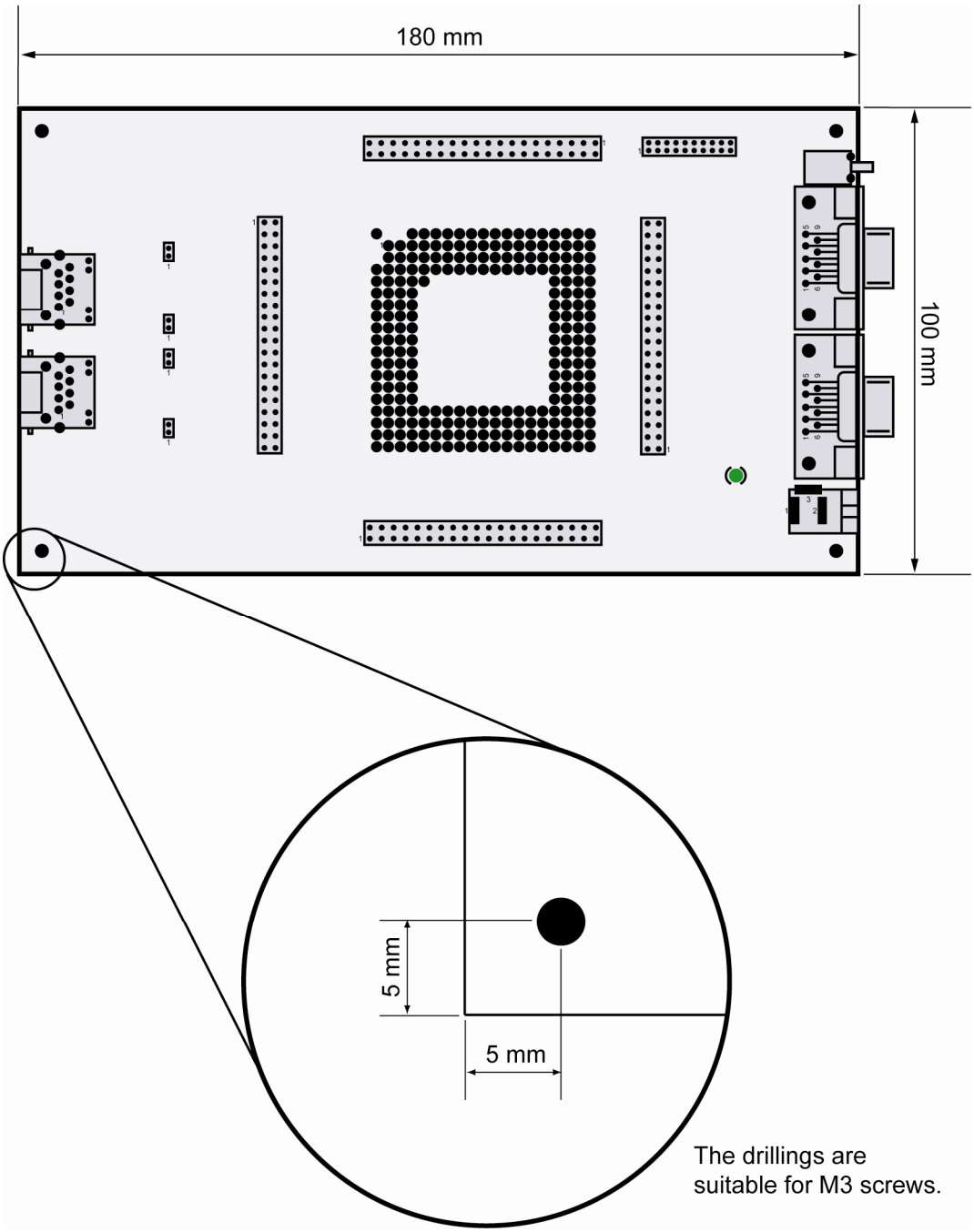


Figure 7: Mechanical dimensions of DNP/EVA8

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DOCUMENT HISTORY

Revision	Date	Remarks	Name
1.0	2005-05-03	first version	WBU

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