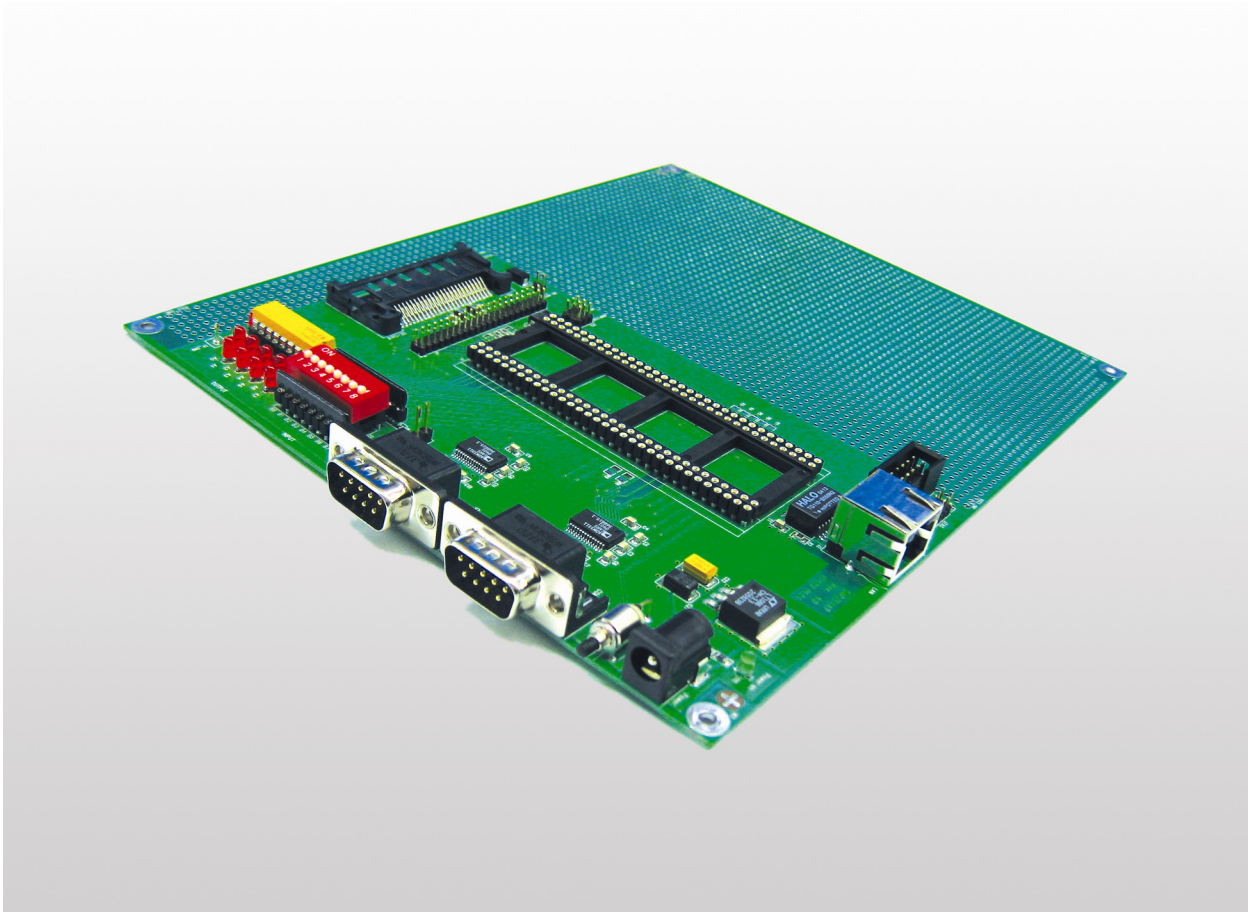
DNP/EVA7

Board Revision 1.0

Hardware Reference



SSV Embedded Systems
Heisterbergallee 72
D-30453 Hannover
Phone +49-(0)511-40000-0
Fax +49-(0)511-40000-40
e-mail: sales@ist1.de

Manual Revision: 1.2
Date: 2004-08-30

For further information regarding our products please visit us at www.ssv-embedded.com

CONTENT

1 INTRODUCTION

This document describes the connectors and jumpers of the DNP/EVA7. For further information about the individual components of this product you may follow the links from our website at *http://www.dilnetpc.com*.

Our Website contains a lot of technical information, which will be updated in regular periods.

1.1 Block Diagram

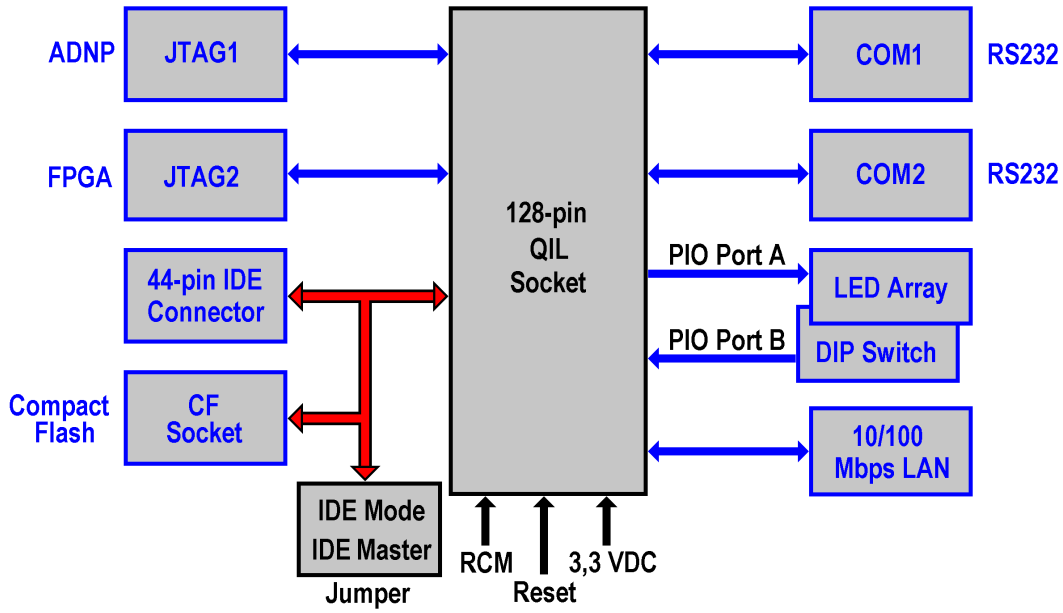
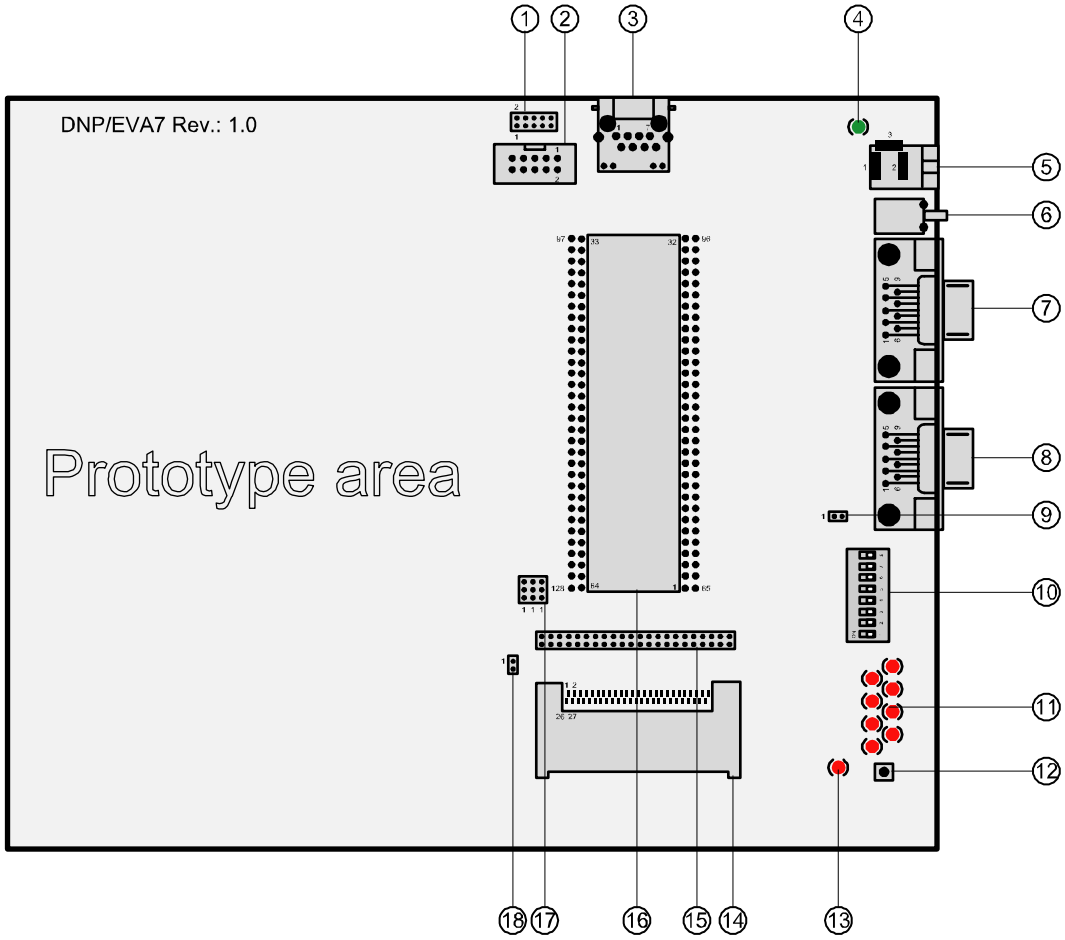


Figure 1-1: DNP/EVA7 block diagram

1.2 Features DNP/EVA7

- QIL-128 Socket for DIL/NetPCs with QIL-128 Pinout
- 2 RS232 serial Ports (COM1 and COM2 of QIL-128 Pinout)
- Array with 8 LEDs on PIO Port A of QIL-128 Pinout
- 8 Position DIP Switch on PIO Port B of QIL-128 Pinout
- DIP Switch and LED Array is removable for freeing Port A and Port B
- RCM Jumper for enable and disable the Remote Console Mode (RCM)
- DIL/NetPC Reset Generation (Power-up Reset, Reset Switch)
- JTAG Connector for standard DIL/NetPC JTAG Interface
- JTAG Connector for FPGA-based DIL/NetPCs
- 44-pin Connector for external IDE devices
- CompactFlash Socket (True IDE Device Support only)
- Mode Jumper for IDE and CompactFlash
- 3.3 VDC Generation from a external 5 VDC Source
- 5V DC supply voltage

2 BOARD LAYOUT



① J3 - JTAG port 1 (ADNP)
② J4 - JTAG port 2 (FPGA)
③ J2 - 10/100 Mbps Ethernet LAN
④ D11 - Power LED
⑤ J9 - Power connector
⑥ S1 - Reset button
⑦ J5 - Serial port COM1
⑧ J6 - Serial port COM2
⑨ JP1 - RCM jumper
⑩ S2 - DIP switches
⑪ D2 to D9 - Output LEDs
⑫ Testpoint GND
⑬ D1 - IDE LED
⑭ J8 - CompactFlash socket
⑮ J7 - 44-pin IDE interface
⑯ J1 - 128-pin QIL socket
⑰ JP2 - IDE mode
⑱ JP3 - IDE master

Figure 2-1: Top view of DNP/EVA7

3 BOARD COMPONENTS

This chapter describes the components of the DNP/EVA7 shown in **chapter 2** and gives a short overview about their respective functions.

3.1 JTAG Port 1 (ADNP) – J3

With this connector you have access to the JTAG interface of the DIL/NetPC mounted on the DNP/EVA7. To use this poart special adapter and software is required. Please contact SSV for further information.

3.2 JTAG Port 2 (FPGA) – J4

This connector offers a special pinout for use with Altera™ Byteblaster. It works only with an ADNP/ESC1 mounted on the DNP/EVA7. Please contact SSV for further information.

3.3 10/100Mbps Ethernet LAN – J2

The LAN interface owns one green LED in the upper left which shows if a LAN link is established.

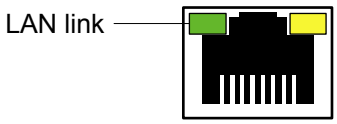


Figure 3-1: LEDs on LAN interface

3.4 Power LED – D11

The green power LED indicates a present supply voltage. This LEDis on when the DNP/EVA7 is provided with 5V DC voltage by power supply. If this LED is off, check the connection between the power supply and the DNP/EVA7.

3.5 Power Connector – J9

The DNP/EVA7 needs a supply voltage of 5V DC to work. In your DNP/EVA7 package you will find a plug-in power supply unit to provide the system with the necessary power.

Caution:

Providing the DNP/EVA7 with a voltage higher than the regular 5V DC ±10% could resolve in damaged board components!

3.6 Reset Button – S1

Press the reset button if the system hangs or you need to restart it. Pressing the reset button will only restart the DIL/NetPC. To reset connected devices, turn off power from the system.

3.7 Serial Port COM1 – J5

The DNP/EVA7 is equipped with a standard RS232 serial interface. The COM1 interface comes with a 9-pin Sub-D male connector. The pin assignment of the COM1 interface is identical to the COM port assignment of a PC so it is possible to use a standard cable.

3.8 Serial Port COM2 – J6

The COM2 interface comes with a 9-pin Sub-D male connector. The COM2 interface does not offer handshake-signals.

3.9 RCM Jumper – JP1

The **RCM (Remote Console Mode)** offers the possibility to control the DIL/NetPC via a terminal program.

Note: The default setting of the RCM jumper is set. Only if the RCM jumper is set you will be able to boot Linux on the DIL/NetPC.

To disable RCM remove the jumper cap of the RCM jumper.

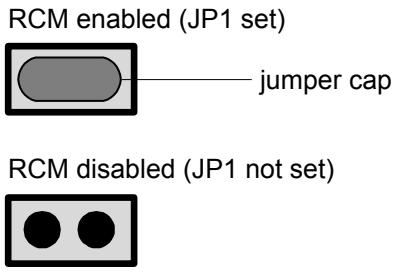


Figure 3-2: Activation of RCM on the DIL/NetPC

3.10 DIP Switches – S2

The DNP/EVA7 has a set of eight DIP switches. The DIP switches give you the possibility to put 8-bit binary numbers to the input ports PB0–PB7.

DIP switch	1	2	3	4	5	6	7	8
PIO bit	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
Switch closed = Signal Vin High (Vcc) Switch open = Signal Vin Low (GND)								

Table 3-1: Assignment of DIP switches

3.11 Output LEDs – D2 to D9

These red LEDs show activity on the output ports PA0–PA7.

Output LED	D2	D3	D4	D5	D6	D7	D8	D9
Port	PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7

Table 3-2: Assignment of output LEDs

3.12 Testpoint Ground

Please connect the ground-pin of your test equipment with the testpoint when you check the board.

3.13 IDE LED – D1

This red LED shows the activity of an IDE-device connected to the IDE interface.

3.14 CompactFlash Socket – J8

With the CompactFlash socket you can connect CF cards to the DNP/EVA7.

Note: The CompactFlash socket works only with CF cards in True-IDE-Mode. The CF cards must be hardwired as master.

Please see **chapter A2.2** and **A2.3** for the complete pinout of the CompactFlash socket.

3.15 44-pin IDE Interface – J7

This IDE interface offers the possibility to connect an IDE-device.

Note: The IDE interface supports only 3.3V devices.

3.16 128-pin QIL Socket – J1

The QIL socket with 128 pins can hold one DIL/NetPC ADNP/1520 or ADNP/ESC1.

3.17 IDE Mode – JP2

Only if you have an ADNP/ESC1 mounted and an IDE-device connected on the DNP/EVA7 you have to change the setting of JP2.

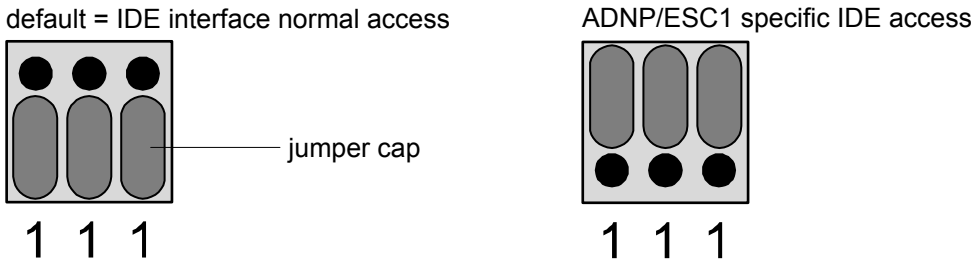


Figure 3-3: Setting of IDE access

3.18 IDE Master – JP3

The jumper JP3 offers the possibility to operate an IDE-device in slave or in master mode.

Note: The default setting of JP3 is set. Only if JP3 is set the IDE-device will work as master.

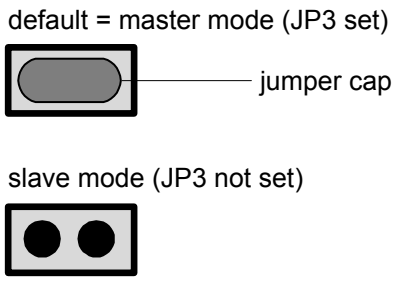


Figure 3-4: Activation of master/slave mode for IDE-device

APPENDIX 1: MECHANICAL DIMENSIONS

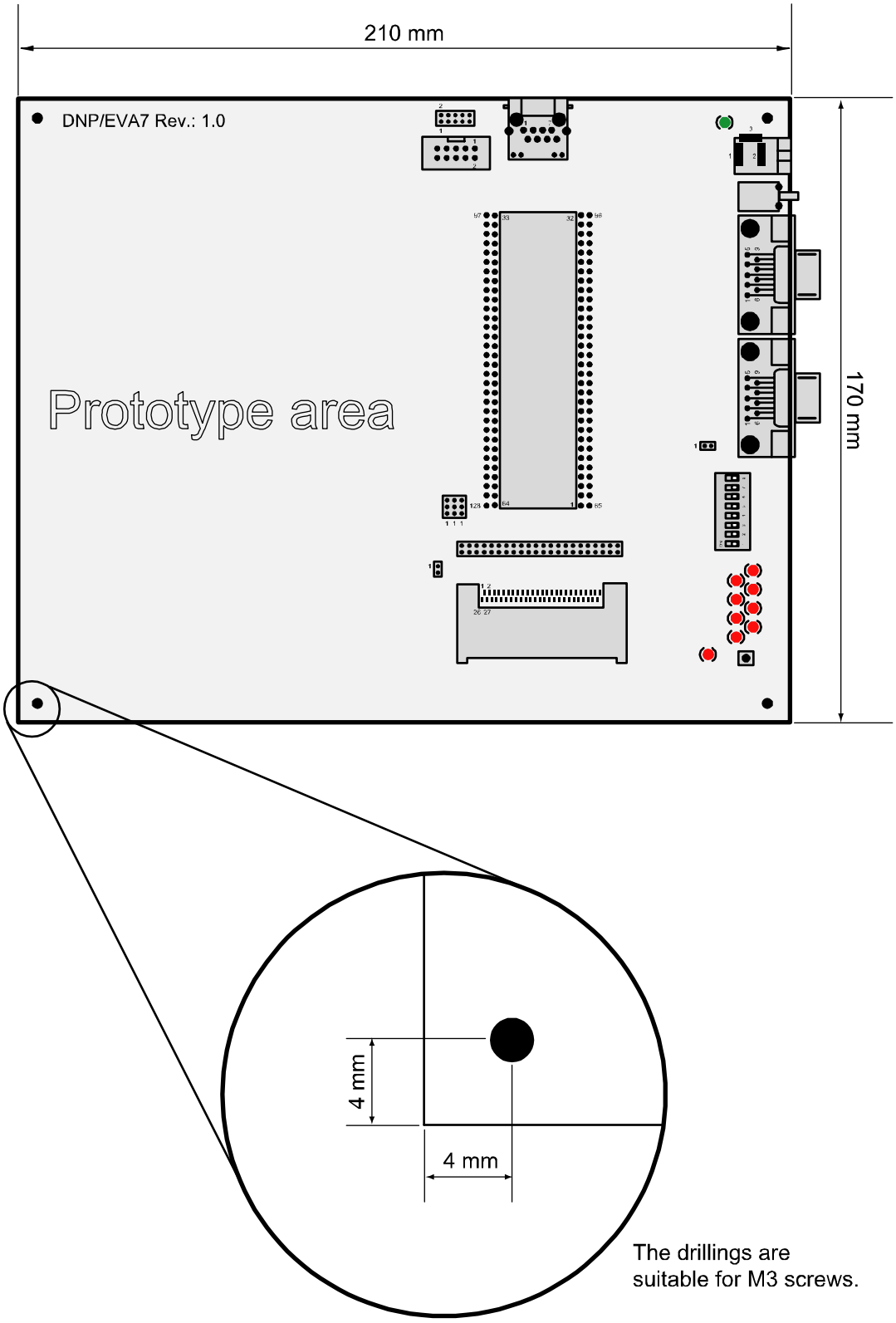


Figure A1-1: Mechanical Dimensions of DNP/EVA7

APPENDIX 2: PIN ASSIGNMENT – 128-PIN QIL SOCKET

A2.1 Pin Assignment - 128-pin QIL Socket J1 (1. Part)

Pin	Name	Group	Function	Used
1	PA0	PIO	Parallel I/O, Port A, Bit 0	Yes
2	PA1	PIO	Parallel I/O, Port A, Bit 1	Yes
3	PA2	PIO	Parallel I/O, Port A, Bit 2	Yes
4	PA3	PIO	Parallel I/O, Port A, Bit 3	Yes
5	PA4	PIO	Parallel I/O, Port A, Bit 4	Yes
6	PA5	PIO	Parallel I/O, Port A, Bit 5	Yes
7	PA6	PIO	Parallel I/O, Port A, Bit 6	Yes
8	PA7	PIO	Parallel I/O, Port A, Bit 7	Yes
9	PB0	PIO	Parallel I/O, Port B, Bit 0	Yes
10	PB1	PIO	Parallel I/O, Port B, Bit 1	Yes
11	PB2	PIO	Parallel I/O, Port B, Bit 2	Yes
12	PB3	PIO	Parallel I/O, Port B, Bit 3	Yes
13	PB4	PIO	Parallel I/O, Port B, Bit 4	Yes
14	PB5	PIO	Parallel I/O, Port B, Bit 5	Yes
15	PB6	PIO	Parallel I/O, Port B, Bit 6	Yes
16	PB7	PIO	Parallel I/O, Port B, Bit 7	Yes
17	PC0	PIO	Parallel I/O, Port C, Bit 0	-
18	PC1	PIO	Parallel I/O, Port C, Bit 1	-
19	PC2	PIO	Parallel I/O, Port C, Bit 2	-
20	PC3	PIO	Parallel I/O, Port C, Bit 3	-
21	RXD1	SIO	COM1 Serial Port, RXD Pin	Yes
22	TXD1	SIO	COM1 Serial Port, TXD Pin	Yes
23	CTS1	SIO	COM1 Serial Port, CTS Pin	Yes
24	RTS1	SIO	COM1 Serial Port, RTS Pin	Yes
25	DCD1	SIO	COM1 Serial Port, DCD Pin	Yes
26	DSR1	SIO	COM1 Serial Port, DSR Pin	Yes
27	DTR1	SIO	COM1 Serial Port, DTR Pin	Yes
28	RI1	SIO	COM1 Serial Port, RI Pin	Yes
29	RESIN	RESET	RESET Input	Yes
30	TX+	LAN	10/100 Mbps Ethernet Interface, TX+ Pin	Yes
31	TX-	LAN	10/100 Mbps Ethernet Interface, TX- Pin	Yes
32	GND	---	Ground	Yes

Table A2-1: 128-pin QIL connector pinout – pin 1 to 32

A2.2 Pin Assignment - 128-pin QIL Connector J1 (2. Part)

Pin	Name	Group	Function	Used
33	RX+	LAN	10/100 Mbps Ethernet Interface, RX+ Pin	Yes
34	RX-	LAN	10/100 Mbps Ethernet Interface, RX- Pin	Yes
35	RESOUT	RESET	RESET Output	-
36	VBAT	PSP*	Real Time Clock Battery Input	-
37	CLKOUT	PSP*	Clock Output (Default 3.6864 MHz)	-
38	TXD2	PSP*	COM2 Serial Port, TXD Pin	Yes
39	RXD2	PSP*	COM2 Serial Port, RXD Pin	Yes
40	INT5	PSP*	Programmable Interrupt Input 5	-
41	INT4	PSP*	Programmable Interrupt Input 4	-
42	INT3	PSP*	Programmable Interrupt Input 3	-
43	INT2	PSP*	Programmable Interrupt Input 2	-
44	INT1	PSP*	Programmable Interrupt Input 1	-
45	CS4	PSP*	Programmable Chip Select Output 4	-
46	CS3	PSP*	Programmable Chip Select Output 3	-
47	CS2	PSP*	Programmable Chip Select Output 2	Yes
48	CS1	PSP*	Programmable Chip Select Output 1	Yes
49	IOCHRDY	PSP*	I/O Channel Ready	Yes
50	IOR	PSP*	I/O Read Signal, I/O Expansion Bus	Yes
51	IOW	PSP*	I/O Write Signal, I/O Expansion Bus	Yes
52	SA3	PSP*	System Expansion Bus, Address Bit 3	Yes
53	SA2	PSP*	System Expansion Bus, Address Bit 2	Yes
54	SA1	PSP*	System Expansion Bus, Address Bit 1	Yes
55	SA0	PSP*	System Expansion Bus, Address Bit 0	Yes
56	SD7	PSP*	System Expansion Bus, Data Bit 7	Yes
57	SD6	PSP*	System Expansion Bus, Data Bit 6	Yes
58	SD5	PSP*	System Expansion Bus, Data Bit 5	Yes
59	SD4	PSP*	System Expansion Bus, Data Bit 4	Yes
60	SD3	PSP*	System Expansion Bus, Data Bit 3	Yes
61	SD2	PSP*	System Expansion Bus, Data Bit 2	Yes
62	SD1	PSP*	System Expansion Bus, Data Bit 1	Yes
63	SD0	PSP*	System Expansion Bus, Data Bit 0	Yes
64	Vcc	---	3.3 Volt Power Input	Yes

* = Product Specific Pins

Table A2-2: 128-pin QIL connector pinout – pin 33 to 64

A2.3 Pin Assignment - 128-pin QIL Connector J1 (3. Part)

Pin	Name	Group	Function	Used
65	SBHE	PSP*	System Byte High Enable, System Expansion Bus	-
66	IOCS16	PSP*	I/O Chip Select 16, System Expansion Bus	Yes
67	Reserved	PSP*	Reserved	-
68	Reserved	PSP*	Reserved	-
69	Reserved	PSP*	Reserved	-
70	BALE	PSP*	Bus Latch Enable, System Expansion Bus	-
71	AEN	PSP*	Address Enable Signal, System Expansion Bus	-
72	Reserved	PSP*	Reserved – Do not use	-
73	RCME	PSP*	Remote Console Mode Enable	Yes
74	Reserved	PSP*	Reserved – Do not use	Yes
75	Reserved	PSP*	Reserved – Do not use	Yes
76	Reserved	PSP*	Reserved – Do not use	Yes
77	Reserved	PSP*	Reserved – Do not use	Yes
78	Reserved	PSP*	Reserved – Do not use	Yes
79	Reserved	PSP*	Reserved – Do not use	Yes
80	Reserved	PSP*	Reserved – Do not use	-
81	Reserved	PSP*	Reserved – Do not use	-
82	Reserved	PSP*	Reserved – Do not use	-
83	Reserved	PSP*	Reserved – Do not use	-
84	Reserved	PSP*	Reserved – Do not use	-
85	INT6	PSP*	Programmable Interrupt Input 6	Yes
86	INT7	PSP*	Programmable Interrupt Input 7	-
87	IDERES	PSP*	IDE Interface Reset Output	Yes
88	IDECS0	PSP*	IDE Interface Chip Select 0	Yes
89	IDECS1	PSP*	IDE Interface Chip Select 1	Yes
90	Reserved	PSP*	Reserved – Do not use	-
91	Reserved	PSP*	Reserved – Do not use	-
92	Reserved	PSP*	Reserved – Do not use	-
93	Reserved	PSP*	Reserved – Do not use	-
94	Reserved	PSP*	Reserved – Do not use	-
95	Reserved	PSP*	Reserved – Do not use	-
96	GND	---	Ground	Yes

* = Product Specific Pins

Table A2-3: 128-pin QIL connector pinout – pin 65 to 96

A2.4 Pin Assignment - 128-pin QIL Connector J1 (4. Part)

Pin	Name	Group	Function	Used
97	LANLED	PSP*	LAN Interface Activty LED	Yes
98	Reserved	PSP*	Reserved – Do not use	-
99	RSTDRV	PSP*	Reset Output, System Expansion Bus	-
100	SA23	PSP*	System Expansion Bus, Address Bit 23	-
101	SA22	PSP*	System Expansion Bus, Address Bit 22	-
102	SA21	PSP*	System Expansion Bus, Address Bit 21	-
103	SA20	PSP*	System Expansion Bus, Address Bit 20	-
104	SA19	PSP*	System Expansion Bus, Address Bit 19	-
105	SA18	PSP*	System Expansion Bus, Address Bit 18	-
106	SA17	PSP*	System Expansion Bus, Address Bit 17	-
107	SA16	PSP*	System Expansion Bus, Address Bit 16	-
108	SA15	PSP*	System Expansion Bus, Address Bit 15	-
109	SA14	PSP*	System Expansion Bus, Address Bit 14	-
110	SA13	PSP*	System Expansion Bus, Address Bit 13	-
111	SA12	PSP*	System Expansion Bus, Address Bit 12	-
112	SA11	PSP*	System Expansion Bus, Address Bit 11	-
113	SA10	PSP*	System Expansion Bus, Address Bit 10	-
114	SA9	PSP*	System Expansion Bus, Address Bit 9	-
115	SA8	PSP*	System Expansion Bus, Address Bit 8	-
116	SA7	PSP*	System Expansion Bus, Address Bit 7	-
117	SA6	PSP*	System Expansion Bus, Address Bit 6	-
118	SA5	PSP*	System Expansion Bus, Address Bit 5	-
119	SA4	PSP*	System Expansion Bus, Address Bit 4	Yes
120	SD15	PSP*	System Expansion Bus, Data Bit 15	Yes
121	SD14	PSP*	System Expansion Bus, Data Bit 14	Yes
122	SD13	PSP*	System Expansion Bus, Data Bit 13	Yes
123	SD12	PSP*	System Expansion Bus, Data Bit 12	Yes
124	SD11	PSP*	System Expansion Bus, Data Bit 11	Yes
125	SD10	PSP*	System Expansion Bus, Data Bit 10	Yes
126	SD9	PSP*	System Expansion Bus, Data Bit 9	Yes
127	SD8	PSP*	System Expansion Bus, Data Bit 8	Yes
128	Vcc	---	3.3 Volt Power Input	Yes

* = Product Specific Pins

Table A2-4: 128-pin QIL connector pinout – pin 97 to 128

APPENDIX 3: PIN ASSIGNMENT OF COMPONENTS

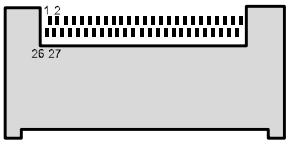
A3.1 Pin Assignment - 44-pin IDE Interface J7

Pin	Name	Function
1	RESET#	IDE_5
2	GND	Power
3	D7	SD7
4	D8	SD8
5	D6	SD6
6	D9	SD9
7	D5	SD5
8	D10	SD10
9	D4	SD4
10	D11	SD11
11	D3	SD3
12	D12	SD12
13	D2	SD2
14	D13	SD13
15	D1	SD1
16	D14	SD14
17	D0	SD0
18	D15	SD15
19	GND	Ground
20	Not connected	---
21	DRQ	---
22	GND	Ground
23	IOW#	IDE_0
24	GND	Ground
25	IOR#	IDE_1
26	GND	Ground
27	RDY	IDE_2
28	SYNC	---
29	DACK#	---
30	GND	Ground
31	IRQ	IDE_6
32	IO16#	IDE_7
33	A1	SA1/3*
34	PDIAG	IDE_8
35	A0	SA0/2*
36	A2	SA2/4*
37	CS0#	IDE_4
38	CS1#	IDE_3
39	DASP#	IDE_9
40	GND	Ground
41	Vcc	Power
42	Vcc	Power
43	GND	Ground
44	Not connected	---

* depends on position of JP2

Table A3-1: 44-pin IDE interface pinout

A3.2 Pin Assignment - CompactFlash Socket J8 (1. Part)

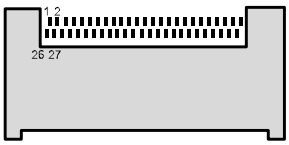
Top view	Pin	Name	Function
	1	GND	Ground
	2	D3	SD3
	3	D4	SD4
	4	D5	SD5
	5	D6	SD6
	6	D7	SD7
	7	CS0#	IDE_4
	8	A10	Ground
	9	ATASEL#	Ground
	10	A9	Ground
	11	A8	Ground
	12	A7	Ground
	13	Vcc	Power
	14	A6	Ground
	15	A5	Ground
	16	A4	Ground
	17	A3	Ground
	18	A2	SA2/4*
	19	A1	SA1/3*
	20	A0	SA0/2*
	21	D0	SD0
	22	D1	SD1
	23	D2	SD2
	24	IOCS16#	IDE_7
	25	CD2#	---

* depends on position of JP2

Table A3-2: Pinout CompactFlash socket – pin 1 to 25

Note: The CompactFlash socket works only with CF cards in True IDE mode. The CF cards must be hardwired as master.

A3.3 Pin Assignment - CompactFlash Socket J8 (2. Part)

Top view	Pin	Name	Function
	26	CD1#	---
	27	D11	SD11
	28	D12	SD12
	29	D13	SD13
	30	D14	SD14
	31	D15	SD15
	32	CS1#	IDE_3
	33	VS1	---
	34	IOR#	IDE_1
	35	IOW#	IDE_0
	36	WE#	Vcc3
	37	IRQ	IDE_6
	38	Vcc	Power
	39	CSEL#	IDE_10
	40	VS2	---
	41	RESET#	IDE_5
	42	IOCHRDY	IDE_2
	43	INPACK#	---
	44	REG#	Vcc3
	45	DASP#	IDE_9
	46	PDIAG#	IDE_8
	47	D8	SD8
	48	D9	SD9
	49	D10	SD10
	50	GND	Ground

* depends on position of JP2

Table A3-3: Pinout CompactFlash socket – pin 26 to 50

Note: The CompactFlash socket works only with CF cards in True IDE mode. The CF cards must be hardwired as master.

A3.4 COM1 Connector J5

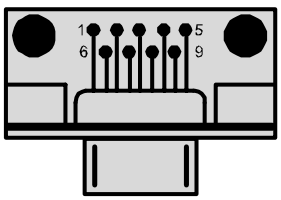
Top view	Pin	Name	Function
	1	DCD	COM1 serial port, DCD pin
	2	RXD	COM1 serial port, RXD pin
	3	TXD	COM1 serial port, TXD pin
	4	DTR	COM1 serial port, DTR pin
	5	GND	Ground
	6	DSR	COM1 serial port, DSR pin
	7	RTS	COM1 serial port, RTS pin
	8	CTS	COM1 serial port, CTS pin
	9	RI	COM1 serial port, RI pin

Table A3-4: Pinout COM1 connector

Note: All COM1-port signals are on RS232 level. There is no TTL level available on this port.

A3.5 COM2 Connector J6

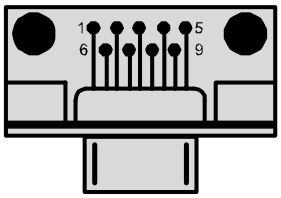
Top view	Pin	Name	Function
	1	---	Not connected
	2	RXD	COM2 serial port, RXD pin
	3	TXD	COM2 serial port, TXD pin
	4	---	Not connected
	5	GND	Ground
	6	---	Not connected
	7	---	Not connected
	8	---	Not connected
	9	---	Not connected

Table A3-5: Pinout COM2 connector

Note: All COM2-port signals are on RS232 level. There is no TTL level available on this port.

A3.6 10/100 Mbps Ethernet Connector J2

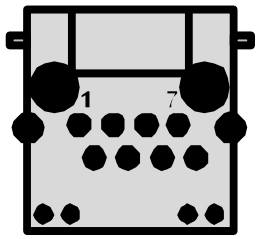
Top view	Pin	Name	Function
	1	TX+	10/100 Mbps LAN, TX+ pin
	2	TX-	10/100 Mbps LAN, TX- pin
	3	RX+	10/100 Mbps LAN, RX+ pin
	4	---	Not connected
	5	---	Not connected
	6	RX-	10/100 Mbps LAN, RX- pin
	7	---	Not connected
	8	---	Not connected

Table A3-6: Pinout 10/100 Mbps Ethernet connector

A3.7 Power Connector J9

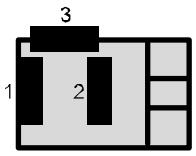
Top view	Pin	Name	Function
	1	Vcc	Power In
	2	GND	Ground
	3	GND	Ground

Table A3-7: Pinout power connector

A3.8 JTAG Port 1 (ADNP) J3

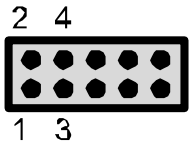
Top view	Pin	Name	Function
	1	JTAG_0	TDI
	2	JTAG_1	TDO
	3	JTAG_2	TMS
	4	GND	Power
	5	JTAG_4	TRST#
	6	JTAG_3	TCK
	7	Vcc3	Power
	8	---	Not connected
	9	JTAG_5	WDdis#
	10	GND	Ground

Table A3-8: Pinout JTAG port 1 (ADNP)

A3.9 JTAG Port 2 (FPGA) J4

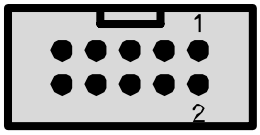
Top view	Pin	Name	Function
	1	JTAG_3	TCK
	2	GND	Ground
	3	JTAG_1	TDO
	4	Vcc3	Power
	5	JTAG_2	TMS
	6	---	Not connected
	7	---	Not connected
	8	---	Not connected
	9	JTAG_0	TDI
	10	GND	Ground

Table A3-9: Pinout JTAG port 2 (FPGA)

CONTACT

SSV Embedded Systems
Heisterbergallee 72
D-30453 Hannover
Phone +49-(0)511-40000-0
Fax +49-(0)511-40000-40
e-mail: sales@ist1.de
Internet: www.ssv-embedded.de

DOCUMENT HISTORY

Revision	Date	Remarks	Name
1.0	2004-06-14	first version	WBU
1.1	2004-07-09	appendix 1 and 2 improved	WBU
1.2	2004-08-30	changed block diagram in chapter 1.1	WBU

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