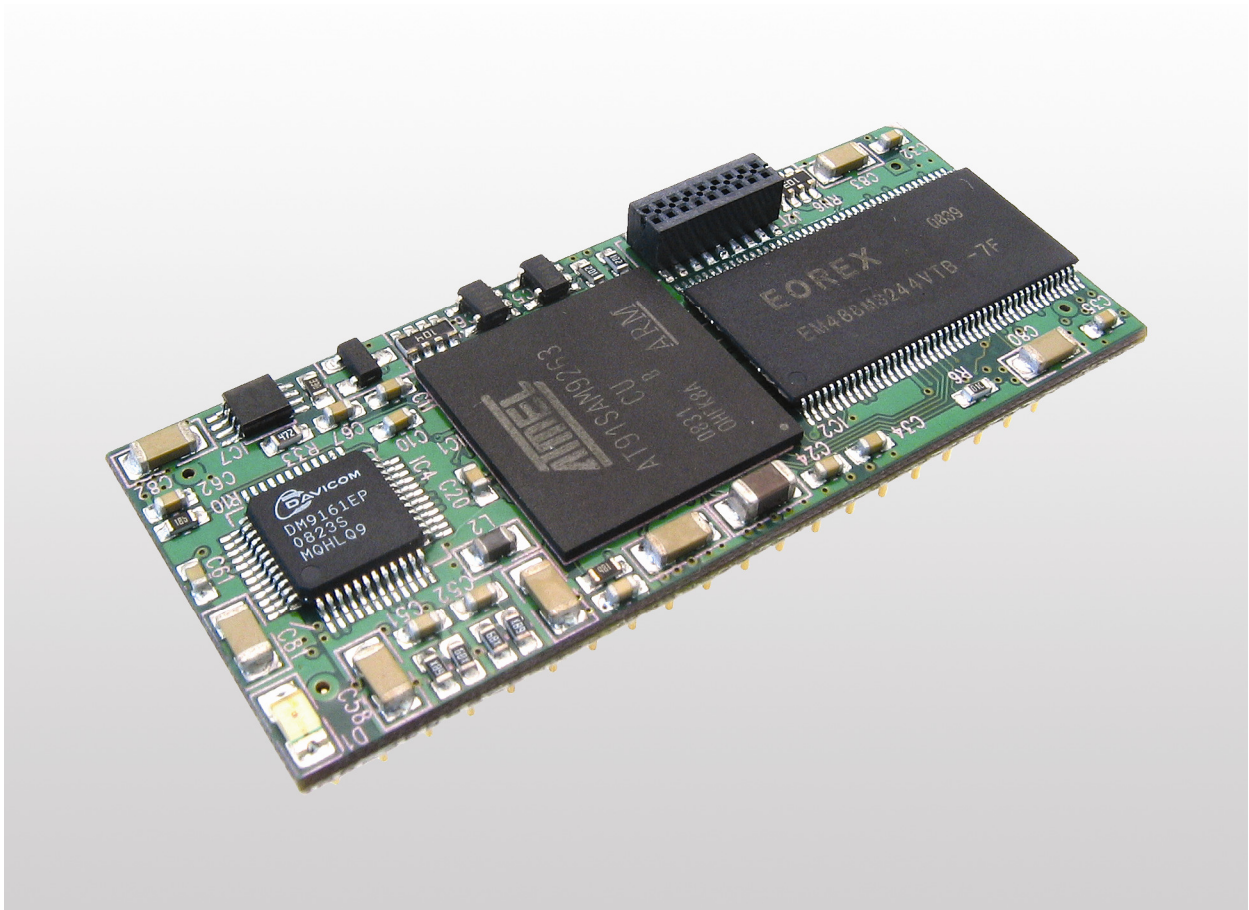


DIL/NetPC DNP/9265

Board Revision 1.0

Hardware Reference



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1 INTRODUCTION

This document describes the hardware components of the DIL/NetPC DNP/9265. For further information about the individual components of this product you may follow the links from our website at <http://www.dilnetpc.com>. Our website contains a lot of technical information, which will be updated in regular periods.

1.1 Safety Guidelines

Please read the following safety guidelines carefully! In case of property or personal damage by not paying attention to this document and/or by incorrect handling, we do not assume liability. In such cases any warranty claim expires.



ATTENTION: Observe precautions for handling – electrostatic sensitive device!

- Discharge yourself before you work with the device, e.g. by touching a heater of metal, to avoid damages.
- Stay grounded while working with the device to avoid damage through electrostatic discharge.

1.2 Conventions

Convention	Usage
bold	Important terms
<i>italic</i>	Filenames, user inputs and command lines
monospace	Pathnames, internet addresses and program code

Table 1: Conventions used in this Document

1.3 Block Diagram

The DIL/NetPC DNP/9265 comes with 1x 10/100 Mbps Ethernet LAN interface, 20-bit GPIO, 1x SPI with master/slave support, 1x I2C interface with master/slave support, 3x UART, 1x CAN controller according to ISO/11898A, 1x SD card interface signals for an external socket and 1x USB 2.0 host port. The DNP/9265 offers a very compact foot print with only 55 mm x 23 mm. The main application area of the DNP/9265 is the field of small size but feature-rich embedded IP gateways for modern industrial, home and laboratory environments.

The DNP/9265 disk drive space for the operating system and the user files is implemented with a 32 MBytes NOR flash chip. This chip contains the pre-installed boot loader and Linux operating system (O/S).

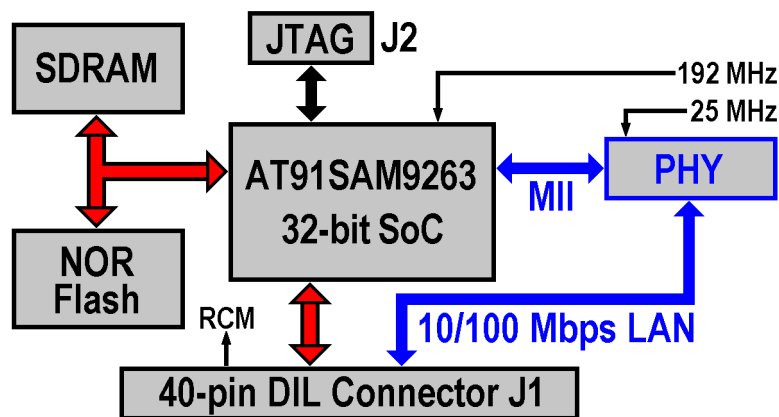


Figure 1: Block diagram of DIL/NetPC DNP/9265

The main component of the DNP/9265 is the 200 MIPS Atmel AT91SAM9263 ARM926EJ-S-based SoC. These SoC employs 27 DMA channels including a 20-channel peripheral DMA controller (PDC), a 9-layer bus matrix, and two additional busses for data- and instruction-tightly-coupled-memories (TCMs) to boost CPU performance and provide on-chip data transfer rates of up to 41.6 Gbps. Two external bus interfaces (EBIs) support gigabyte-plus external memories. On the DNP/9265 the AT91SAM9263 runs with 192 MHz.

1.4 Features and Technical Data

- AT91SAM9263 32-bit ARM9 SoC @ 192 MHz
- 32 MByte SDRAM
- 32 MByte NOR-type flash device
- 1x 10/100 Mbps Ethernet LAN interface
- 20-bit GPIO (General Purpose Input Output)
- 3x UART (COM1 with all hardware handshake signals, COM2 TX/RX only, COM3 TX/RX/RTS/CTS - functional OR with four GPIO signals)
- 1x SPI master/slave controller, functional OR with four GPIO signals
- 1x I2C interface master/slave controller, functional OR with two GPIO signals
- 1x ISO/11898A 2.0B CAN controller
- 1x USB 2.0 host port with FS and LS support
- 1x SD card interface signals for external socket functional OR with GPIO signals
- Programmable watchdog timer
- Power supervisor for VCC control
- 40-pin JEDEC DIL-40 connector, 2.54 mm centers
- Pin-compatible to other SSV DIL-40 devices
- Supply voltage 3.3 VDC ($\pm 5\%$)
- Supply current 300 mA typical / 500 mA max.
- Size 55 mm x 23 mm
- Preinstalled U-Boot boot loader with flash device support
- Preinstalled Linux O/S with 2.6.24 kernel (**see note 1**)

Note 1: The DNP/9265 Linux O/S is based on the OpenEmbedded software framework.

2 BOARD LAYOUT

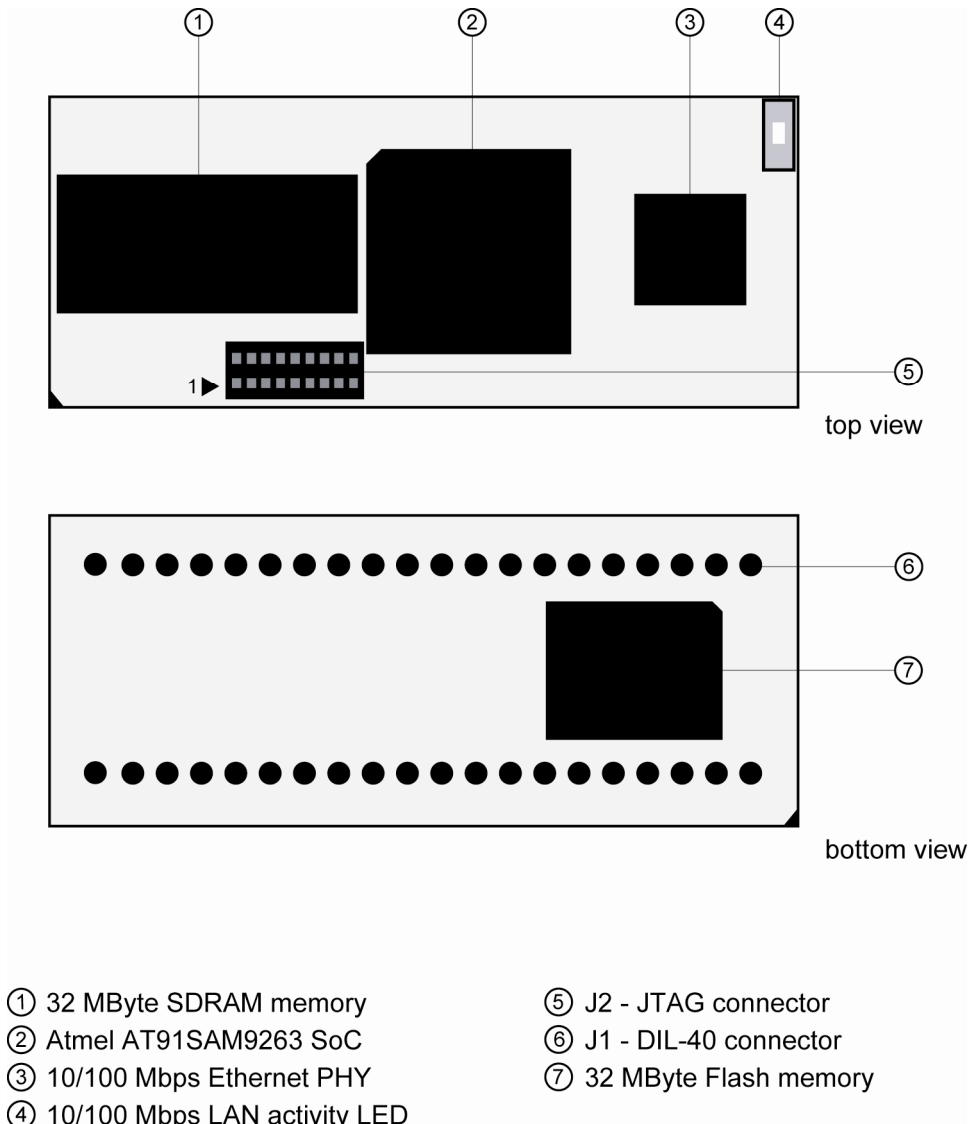


Figure 2: Board layout DIL/NetPC DNP/9265

3 PINOUTS

3.1 DIL-40 Connector – J1

Pin	Name	Group	Function
1	PA0	PIO	Parallel I/O, Port A, Bit 0
2	PA1	PIO	Parallel I/O, Port A, Bit 1
3	PA2	PIO	Parallel I/O, Port A, Bit 2
4	PA3	PIO	Parallel I/O, Port A, Bit 3
5	PA4	PIO	Parallel I/O, Port A, Bit 4
6	PA5	PIO	Parallel I/O, Port A, Bit 5
7	PA6	PIO	Parallel I/O, Port A, Bit 6
8	PA7	PIO	Parallel I/O, Port A, Bit 7
9	PB0	PIO	Parallel I/O, Port B, Bit 0
10	PB1	PIO	Parallel I/O, Port B, Bit 1
11	PB2	PIO	Parallel I/O, Port B, Bit 2
12	PB3	PIO	Parallel I/O, Port B, Bit 3
13	PB4	PIO	Parallel I/O, Port B, Bit 4
14	PB5	PIO	Parallel I/O, Port B, Bit 5
15	PB6	PIO	Parallel I/O, Port B, Bit 6
16	PB7	PIO	Parallel I/O, Port B, Bit 7
17	RESIN	RESET	Reset Input (Low Active)
18	HDMA	USB	USB Host Port -
19	HDPA	USB	USB Host Port +
20	GND	---	Ground
21	RCM	---	RCM (Remote Console Mode) Input
22	TX+	LAN	10/100 Mbps LAN, TX+ Pin
23	TX-	LAN	10/100 Mbps LAN, TX- Pin
24	RX+	LAN	10/100 Mbps LAN, RX+ Pin
25	RX-	LAN	10/100 Mbps LAN, RX- Pin
26	TXD2	SIO	COM2 Serial Port, TXD Pin
27	RXD2	SIO	COM2 Serial Port, RXD Pin
28	RI1	SIO	COM1 Serial Port, RI Pin
29	DTR1	SIO	COM1 Serial Port, DTR Pin
30	DSR1	SIO	COM1 Serial Port, DSR Pin
31	DCD1	SIO	COM1 Serial Port, DCD Pin
32	RTS1	SIO	COM1 Serial Port, RTS Pin
33	CTS1	SIO	COM1 Serial Port, CTS Pin
34	TXD1	SIO	COM1 Serial Port, TXD Pin
35	RXD1	SIO	COM1 Serial Port, RXD Pin
36	PC0	PIO	Parallel I/O, Port C, Bit 0
37	PC1	PIO	Parallel I/O, Port C, Bit 1
38	PC2	PIO	Parallel I/O, Port C, Bit 2
39	PC3	PIO	Parallel I/O, Port C, Bit 3
40	VCC	---	3.3 Volt Power Input

Table 2: Pinout DIL-40 connector

Note: The arrangement of the signals in groups has compatibility reasons. Other products of SSV with DIL-40 pinout are fully or conditionally pin compatible to the DIL/NetPC DNP/9265 by observance of the corresponding application note.

3.2 DIL-40 Connector Function Multiplexing

Some pins of the DIL-40 connector of the DNP/9265 have multiple meanings. The pins have a main and an alternate function (function multiplexing).

The main functions correspond with the standard pinout of the DIL-40 connector as shown in **table 2**. The alternate functions are shown in **table 3** below.

Pin	Name	Main Function	Name	Alternate Function
1	PA0	Parallel I/O, Port A, Bit 0	SDCCLK	SD Card Clock
2	PA1	Parallel I/O, Port A, Bit 1	SDCCMD	SD Card Command
3	PA2	Parallel I/O, Port A, Bit 2	SDCD0	SD Card Data Bit 0
4	PA3	Parallel I/O, Port A, Bit 3	SDCD1	SD Card Data Bit 1
5	PA4	Parallel I/O, Port A, Bit 4	SDCD2	SD Card Data Bit 2
6	PA5	Parallel I/O, Port A, Bit 5	SDCD3	SD Card Data Bit 3
7	PA6	Parallel I/O, Port A, Bit 6	SDCD	SD Card Card Detection
8	PA7	Parallel I/O, Port A, Bit 7	SDCPWR	SD Card Power
9	PB0	Parallel I/O, Port B, Bit 0	TXD3	COM3 Serial Port, TXD Pin
10	PB1	Parallel I/O, Port B, Bit 1	RXD3	COM3 Serial Port, RXD Pin
11	PB2	Parallel I/O, Port B, Bit 2	RTS3	COM3 Serial Port, RTS Pin
12	PB3	Parallel I/O, Port B, Bit 3	CTS3	COM3 Serial Port, CTS Pin
13	PB4	Parallel I/O, Port B, Bit 4	SCL	I2C Clock
14	PB5	Parallel I/O, Port B, Bit 5	SDA	I2C Data
15	PB6	Parallel I/O, Port B, Bit 6	CANTX	CAN Port, TXD Pin
16	PB7	Parallel I/O, Port B, Bit 7	CANRX	CAN Port, RXD Pin
36	PC0	Parallel I/O, Port C, Bit 0	MOSI	SPI MOSI
37	PC1	Parallel I/O, Port C, Bit 1	MISO	SPI MISO
38	PC2	Parallel I/O, Port C, Bit 2	SPICLK	SPI Clock
39	PC3	Parallel I/O, Port C, Bit 3	SPICS0	SPI Chip Select 0

Table 3: DNP/9265 function multiplexing

3.3 JTAG Connector – J2

You can use an adapter to convert the miniature JTAG connector of the DNP/9265 to the common 2.54 mm raster. Then standard JTAG connector modules can be used.

Manufacturer of the JTAG connector (1 mm grid / 2 lines / 2 x 9 pins) is W+P Products (<http://www.wppro.com>), type 7091-18-10-ST.

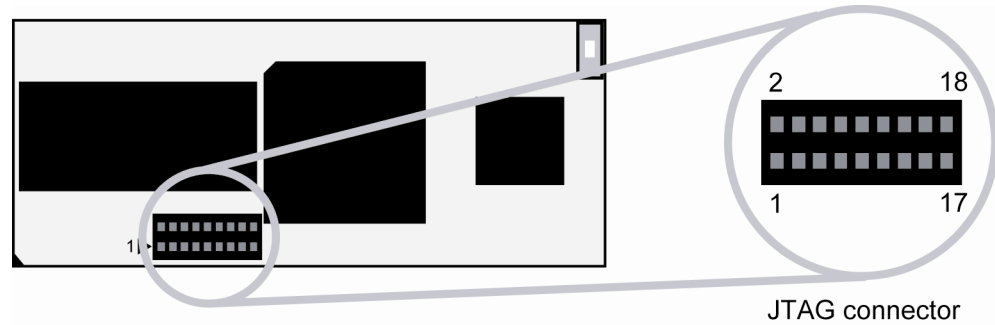


Figure 3: Position of JTAG connector on the DNP/9265

Pin	Name	Function
1	VCC	3.3 VDC I/O Voltage
2	GND	Ground
3	TRST#	Test Reset
4	BMS	Boot Mode Select
5	TDI	Test Data In
6	DTXD	Debug Port TXD
7	TMS#	Test Mode Select
8	DRXD	Debug Port RXD
9	TCK	Test Clock
10	GND	Ground
11	RTCK	Return Clock
12	DDP	USB Device Port +
13	TDO	Test Data Out
14	DDM	USB Device Port -
15	RESET#	Reset
16	---	Not Connected
17	GND	Ground
18	---	Not Connected

Table 4: Pinout JTAG connector

3.4 JTAG Interface

The JTAG signals of the DNP/9265 connector J2 are directly connected to the JTAG TAP controller of the AT91SAM9263 32-bit ARM SoC.

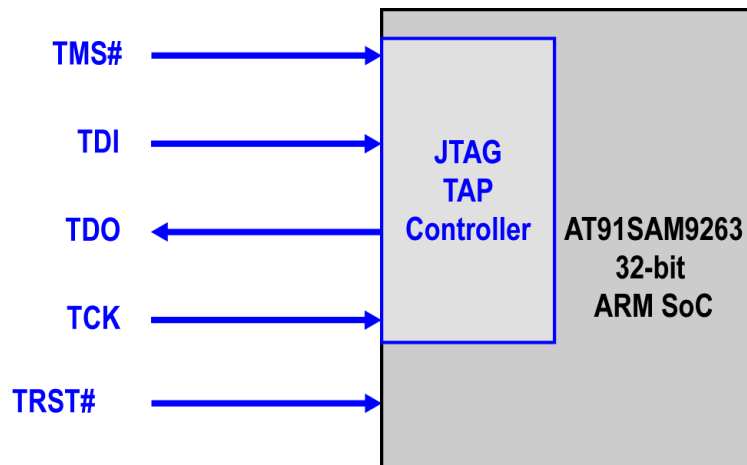


Figure 4: DNP/9265 JTAG interface

4 MECHANICAL DIMENSIONS

All length dimensions have a tolerance of 0.5 mm.

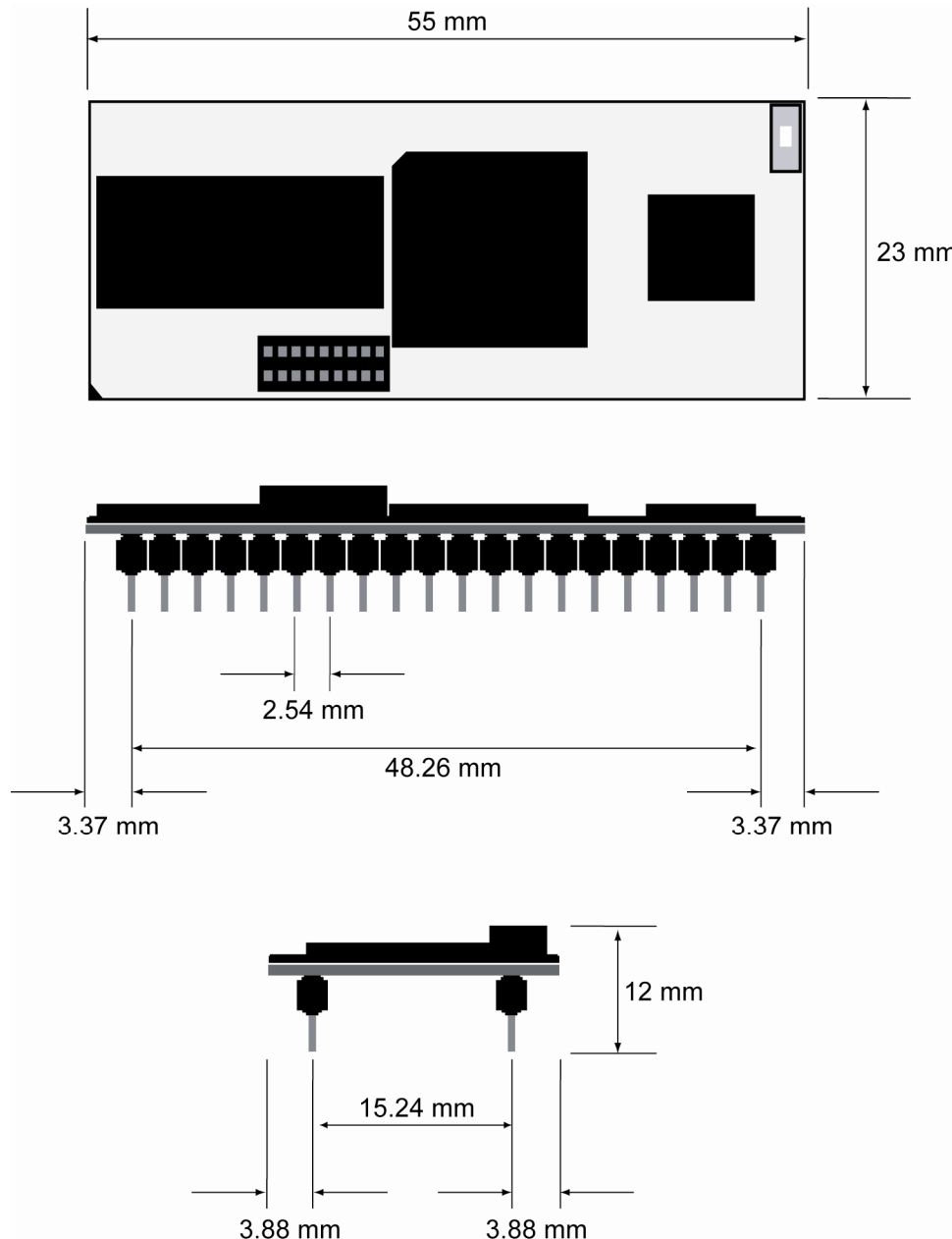


Figure 5: Mechanical dimensions of DIL/NetPC DNP/9265

5 HELPFUL LITERATURE

- AT91SAM9263 Preliminary www.atmel.com
- AT91SAM9263 Preliminary Summary www.atmel.com
- •ARM926EJ-S Technical Reference manual www.atmel.com
- DNP/EVA6 Hardware Reference www.dilnetpc.com

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For actual information about the DIL/NetPC DNP/9265 visit us at www.dilnetpc.com.

DOCUMENT HISTORY

Revision	Date	Remarks	Name
1.0	2009-05-15	first version	WBU
1.1	2010-03-23	corrected table 2 (pins 18 + 19), changed contact information	WBU
1.2	2012-12-07	corrected figure 2	WBU

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