DIL/NetPC DNP/2110
Board Revision 1.0

Hardware Reference

SSV Embedded Systems
Heisterbergallee 72
D-30453 Hannover
Phone +49-(0)511-40000-0
Fax +49-(0)511-40000-40
E-mail: sales@ist1.de

Manual Revision: 1.0
Date: 2004-09-10

For further information regarding our products please visit us at www.dilnetpc.com

CONTENT

1 INTRODUCTION

Thank you for choosing a SSV Product. We are confident that you will be pleased with the performance of your product. Please take a few minutes to read this manual.

For further information about the individual components you may follow the links from our website at: *http://www.dilnetpc.com*

Our Website contains a lot of technical information, which will be updated in regular periods.

1.1 Block Diagram

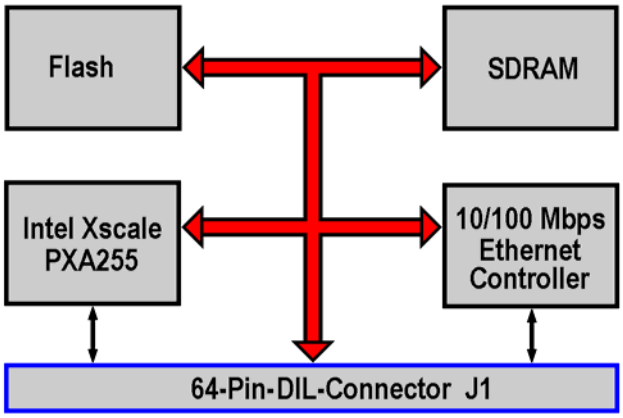
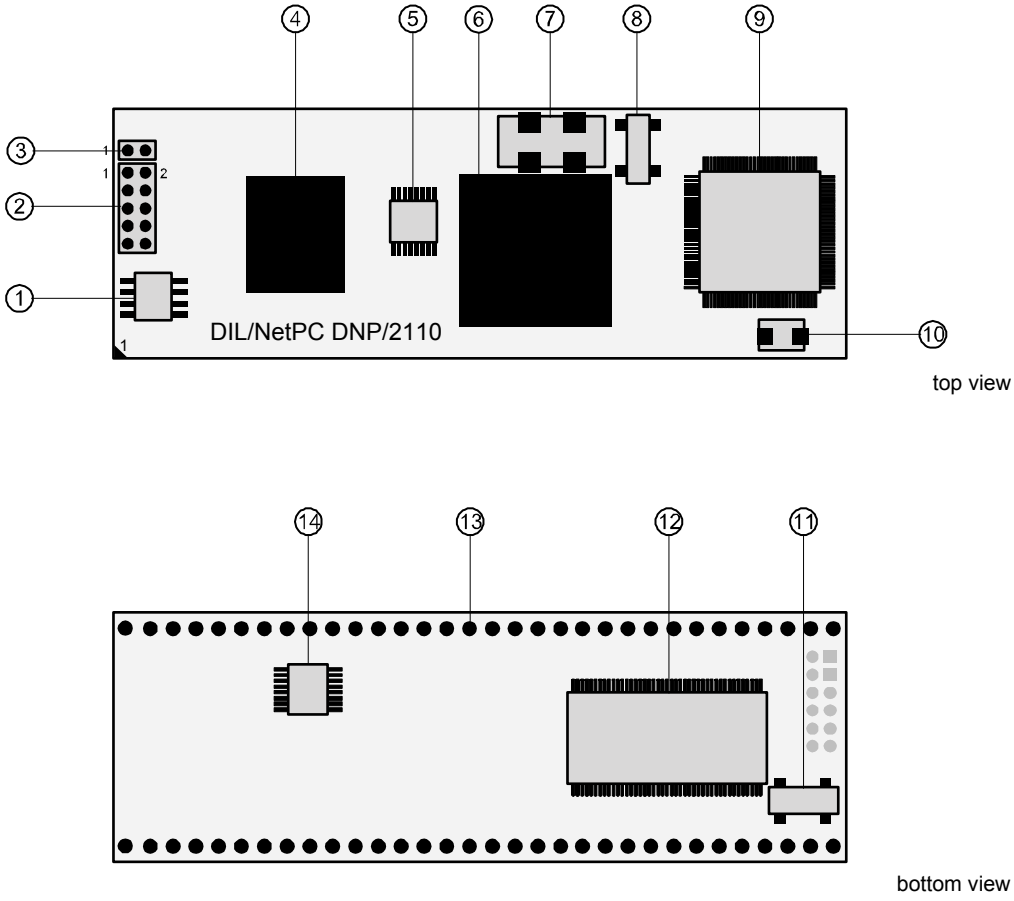


Figure 1-1: Block diagram of the DNP/2110

1.2 Features

- Intel Xscale PXA255 CPU with 400 MHz Clock Speed
- 480 MIPS Dhrystone 2.1 (depends on compiler type and version)
- 397.31 Linux BogoMIPS at 400 MHz
- 16 MByte 32-bit SDRAM Memory, 16 MByte FLASH Memory
- 10/100 Mbps Ethernet Interface
- Two 16550 Serial Ports (one with all Handshakes)
- 20-bit General Purpose high-speed Parallel I/O
- 8-bit I/O Expansion Bus
- 5 Interrupt Inputs, 4 Chip Select Outputs
- Programmable Watchdog Timer
- JTAG IEEE 1149.1 Test Interface
- In-System Programming Features
- 64-pin JEDEC DIL-64 Connector, 2.54mm Centers
- 3.3 Volt Low Power Design, Supply Voltage 3.3 VDC (± 5%)
- Supply Current 300 mA typ. at 400 MHz
- Size 82mm x 28mm

2 DNP/2110 OVERVIEW



① External RTC
② J2 - CPU-JTAG / Service port
③ JP1 - RCM jumper
④ Flash memory
⑤ CPU-core voltage regulator
⑥ GDPXA255-E400 CPU
⑦ 3.6864MHz quartz for CPU
⑧ 32KHz quartz for internal RTC
⑨ 10/100 Mbps Ethernet controller
⑩ 25MHz quartz for Ethernet controller
⑪ 32KHz quartz for external RTC
⑫ SDRAM
⑬ J1 - 64-pin DIL connector
⑭ TTL

Figure 2-1: OverviewDNP/2110

3 DNP/2110 COMPONENTS

This chapter describes components of the DIL/NetPC DNP/2110 shown in **chapter 2** and gives a short overview about their respective functions.

3.1 External RTC

The DS1302 is the external RTC (Real Time Clock) circuit.

3.2 J2 – CPU-JTAG / Service Port

This connector implements the interface to the DNP/2110 JTAG functions.

Please refer to **chapter 4.6** for the complete pinout.

3.3 JP1 – RCM-Jumper

The **RCM (Remote Console Mode)** offers the possibility to control the DNP/2110 via a terminal program.

Note: The default setting of the RCM jumper is set. If you set the RCM jumper you will be able to update the Linux system on the DNP/2110.

To disable RCM remove the jumper cap of the RCM jumper.

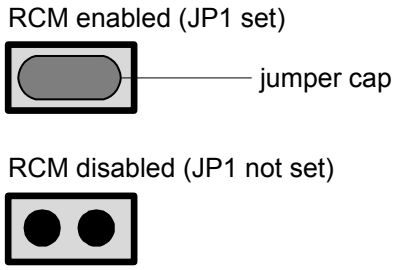


Figure 3-1: Activation of RCM on the DNP/2110

3.4 Flash Memory

The 16MB Flash memory provides storage for the DNP/2110 operating system. The Flash memory is in-system programmable over JTAG, serial and the Ethernet interface.

The boot block of the Flash memory is only in-system programmable over the JTAG interface through a special cable attached to a PC parallel port.

For all other Flash blocks, you can use also a high-speed serial connection through the DNP/2110 COM1 port or the 10/100 Mbps Ethernet interface for in-system programming.

3.5 CPU-Core Voltage Regulator

The MAX1793EUE regulates the CPU-core voltage to 1.3V.

3.6 GDPXA255-E400 CPU

The DNP/2110 provides a very compact Intel 400 MHz PXA255 Xscale-based low power embedded controller with TCP/IP stack and web server for high-speed embedded networking applications.

3.7 3.6864MHz Quartz for CPU

This 3.6864MHz quartz is used by the CPU.

3.8 32KHz Quartz for internal RTC

This 32KHz quartz is used by the internal RTC (Real Time Clock) within the CPU.

3.9 10/100Mbps Ethernet Controller

The 10/100 Mbps Ethernet controller is a SMSC LAN91C111 single chip MAC+PHY.

This highly-integrated Ethernet LAN controller includes 8 KByte internal memory for receive and transmit FIFO buffers, a IEEE 802.3/802.3u Ethernet MAC engine, and internal 10BASE-T and 100BASE-TX transmit and receive filters.

The SMSC LAN91C111 supports full-duplex switched Ethernet operation and auto negotiation for 10 and 100 Mbps.

3.10 25MHz Quartz for Ethernet Controller

This 25MHz quartz is used by the LAN controller.

3.11 32KHz Quartz for external RTC

This 32KHz quartz is used by the external RTC (Real Time Clock).

3.12 SDRAM

The capacity of the SDRAM memory chip is 16 MByte with a 32-bit data path.

3.13 TTL

The 74AHC138 circuit is used for generating external chip selects.

3.14 J1 – 64-pin DIL Connector

The mechanical interface between the DNP/2110 and existing devices and equipment is a JEDEC 64-pin DIL connector with 2.54mm centers. This allows the direct integration to a standard 64-pin DIL socket.

Please refer to **chapter 4.2 and 4.3** for the complete pinout.

4 THE DNP/2110 IN DETAIL

4.1 Mechanical Dimensions

The DNP/2110 uses a 64-pin DIL socket as mechanical base. Figure 4-1 shows the dimensions. All length dimensions have a tolerance of 0.5 mm.

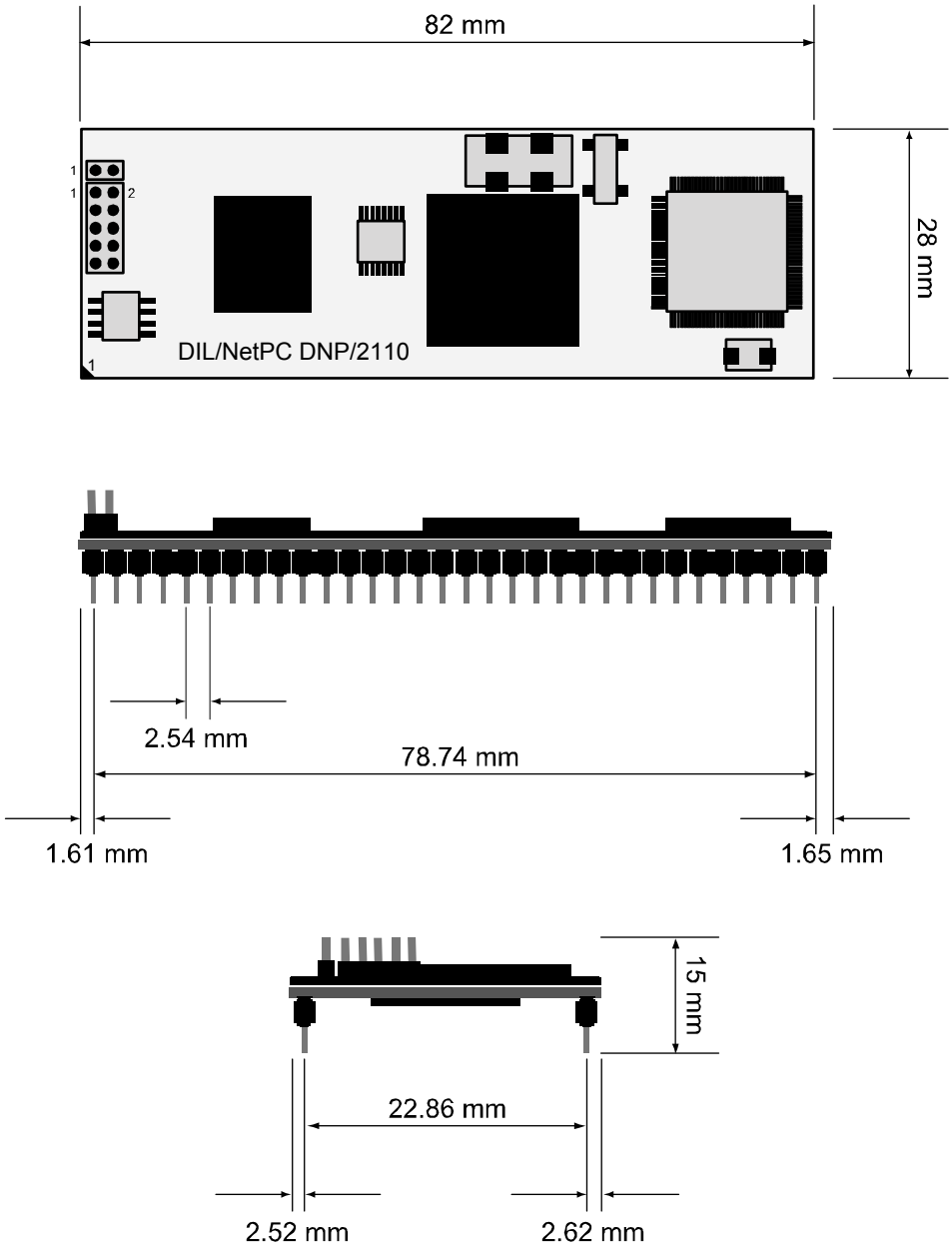


Figure 4-1: Mechanical dimensions of the DNP/2110

4.2 Pin Assignment 64-pin DIL Connector – J1 (1. Part)

Pin	Name	Group	Function
1	PA0	PIO	Parallel I/O, Port A, Bit 0
2	PA1	PIO	Parallel I/O, Port A, Bit 1
3	PA2	PIO	Parallel I/O, Port A, Bit 2
4	PA3	PIO	Parallel I/O, Port A, Bit 3
5	PA4	PIO	Parallel I/O, Port A, Bit 4
6	PA5	PIO	Parallel I/O, Port A, Bit 5
7	PA6	PIO	Parallel I/O, Port A, Bit 6
8	PA7	PIO	Parallel I/O, Port A, Bit 7
9	PB0	PIO	Parallel I/O, Port B, Bit 0
10	PB1	PIO	Parallel I/O, Port B, Bit 1
11	PB2	PIO	Parallel I/O, Port B, Bit 2
12	PB3	PIO	Parallel I/O, Port B, Bit 3
13	PB4	PIO	Parallel I/O, Port B, Bit 4
14	PB5	PIO	Parallel I/O, Port B, Bit 5
15	PB6	PIO	Parallel I/O, Port B, Bit 6
16	PB7	PIO	Parallel I/O, Port B, Bit 7
17	PC0	PIO	Parallel I/O, Port C, Bit 0 (Alternate Function: MOSI (SPI Mode))
18	PC1	PIO	Parallel I/O, Port C, Bit 1 (Alternate Function: MISO (SPI Mode))
19	PC2	PIO	Parallel I/O, Port C, Bit 2 (Alternate Function: SPICLK (SPI Mode))
20	PC3	PIO	Parallel I/O, Port C, Bit 3 (Alternate Function: SPICS (SPI Mode))
21	RXD1	SIO	COM1 Serial Port, RXD Pin
22	TXD1	SIO	COM1 Serial Port, TXD Pin
23	CTS1	SIO	COM1 Serial Port, CTS Pin
24	RTS1	SIO	COM1 Serial Port, RTS Pin
25	DCD1	SIO	COM1 Serial Port, DCD Pin
26	DSR1	SIO	COM1 Serial Port, DSR Pin
27	DTR1	SIO	COM1 Serial Port, DTR Pin
28	RI1	SIO	COM1 Serial Port, RI Pin
29	RESIN	RESET	Reset Input
30	TX+	LAN	10/100 Mbps LAN, TX+ Pin
31	TX-	LAN	10/100 Mbps LAN, TX- Pin
32	GND	----	Ground

Table 4-1: DNP/2110 Pinout – Pin 1 to 32

Please Note: The DNP/2110 PIO port C pins (PC.0, PC.1, PC.2 and PC.3) offer as alternate function SPI mode operation. The DNP/2110 can act as SPI master or SPI slave device. In SPI master mode MOSI (PC.0) is an output, MISO (PC.1) is an input, SPICLK (PC.2) is an output and SPICS (PC.3) is an output. In SPI slave mode MOSI is an input, MISO is an output, SPICLK is an input and SPICS is an input.

4.3 Pin Assignment 64-pin DIL Connector – J1 (2. Part)

Pin	Name	Group	Function
33	RX+	LAN	10/100 Mbps LAN, RX+ Pin
34	RX-	LAN	10/100 Mbps LAN, RX- Pin
35	RESOUT	RESET	Reset Output
36	VBAT	PSP (Product Specific Pins)	Real Time Clock Battery
37	CLKOUT	PSP (Product Specific Pins)	Clock Output (Default 3.6864MHz)
38	TXD2	PSP (Product Specific Pins)	COM2 Serial Port, TXD Pin
39	RXD2	PSP (Product Specific Pins)	COM2 Serial Port, RXD Pin
40	INT5	PSP (Product Specific Pins)	Interrupt Input 5
41	INT4	PSP (Product Specific Pins)	Interrupt Input 4
42	INT3	PSP (Product Specific Pins)	Interrupt Input 3
43	INT2	PSP (Product Specific Pins)	Interrupt Input 2
44	INT1	PSP (Product Specific Pins)	Interrupt Input 1
45	CS4	PSP (Product Specific Pins)	Chip Select Output 4
46	CS3	PSP (Product Specific Pins)	Chip Select Output 3
47	CS2	PSP (Product Specific Pins)	Chip Select Output 2
48	CS1	PSP (Product Specific Pins)	Chip Select Output 1
49	RDY	PSP (Product Specific Pins)	External Ready Input
50	RD	PSP (Product Specific Pins)	Read Signal, Expansion Bus
51	WR	PSP (Product Specific Pins)	Write Signal, Expansion Bus
52	SA3	PSP (Product Specific Pins)	Expansion Bus Address Bit 3
53	SA2	PSP (Product Specific Pins)	Expansion Bus Address Bit 2
54	SA1	PSP (Product Specific Pins)	Expansion Bus Address Bit 1
55	SA0	PSP (Product Specific Pins)	Expansion Bus Address Bit 0
56	SD7	PSP (Product Specific Pins)	Expansion Bus Data Bit 7
57	SD6	PSP (Product Specific Pins)	Expansion Bus Data Bit 6
58	SD5	PSP (Product Specific Pins)	Expansion Bus Data Bit 5
59	SD4	PSP (Product Specific Pins)	Expansion Bus Data Bit 4
60	SD3	PSP (Product Specific Pins)	Expansion Bus Data Bit 3
61	SD2	PSP (Product Specific Pins)	Expansion Bus Data Bit 2
62	SD1	PSP (Product Specific Pins)	Expansion Bus Data Bit 1
63	SD0	PSP (Product Specific Pins)	Expansion Bus Data Bit 0
64	Vcc	---	3.3 Volt Power Input

Table 4-2: DNP/2110 Pinout – Pin 33 to 64

Please Note: Some pins are called "Product Specific Pins (PSP)". Future versions of the DIL/NetPC will differ only with this pins from the DNP/2110. All other pins will have the same functions.

4.4 CPU-JTAG – J2

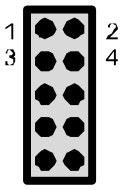
Top view	Pin	Name	Function
	1	TDI	JTAG Serial DataIn
	2	TDO	JTAG Serial DataOut
	3	TMS	JTAG ModeSelect
	4	GND	Ground
	5	TRST#	JTAG Reset
	6	TCK	JTAG Serial clock
	7	Vcc	Power
	8	---	Not connected
	9	---	Not connected
	10	GND	Ground

Table 4-3: Pinout JTAG J2

4.5 RCM-Jumper – JP1

Jumper	Function
open	Disable Remote Console Mode
closed	Enable Remote Console Mode

Table 4-3: Jumper settings RCM – JP1

4.6 COM Port Pin Mapping

The 10 pins of the two DIL/NetPC DNP/2110 UARTs (Serial Ports COM1 and COM2) are direct connected to signals of the Intel PXA255 Xscale 32-bit micro-controller. The following table shows this mapping.

Pin	Name	PXA255 Pin Function	PXA255 Pin	Source
21	RXD1	FFRXD	A13	UART
22	TXD1	FFTXD	E13	UART
23	CTS1	FFCTS	A14	UART
24	RTS1	FFRTS	F8	UART
25	DCD1	FFDCD	A12	UART
26	DSR1	FFDSR	B11	UART
27	DTR1	FFDTR	F10	UART
28	RI1	FFRI	B10	UART
38	TXD2	BTTXD	D13	UART
39	RXD2	BTRXD	B13	UART

Table 4-4: DNP/2110 COM port pin mapping to PXA255 pins

Please see also the *Intel PXA255 Processor Developer's Manual* and the *Intel PXA255 Processor Data Sheet* for the PXA255 pin function details.

4.7 PIO Pin Mapping

The bits of the DNP/2110 20-bit PIO (Parallel Input Output Port) are directly connected to signals of the Intel PXA255 Xscale 32-bit microcontroller. The following table shows this mapping. Please see also the Intel PXA255 Processor Developer's Manual and the Intel PXA255 Processor Data Sheet for the PXA255 pin function details.

Pin	Name	PXA255 Pin Function	PXA255 Pin
1	PA0	GPIO 2	L13
2	PA1	GPIO 3	K14
3	PA2	GPIO 4	I12
4	PA3	GPIO 5	J11
5	PA4	GPIO 6	H14
6	PA5	GPIO 7	G15
7	PA6	GPIO 8	F14
8	PA7	GPIO 9	F12
9	PB0	GPIO 23	F9
10	PB1	GPIO 24	E9
11	PB2	GPIO 25	D9
12	PB3	GPIO 26	A9
13	PB4	GPIO 27	B9
14	PB5	GPIO 28	C9
15	PB6	GPIO 29	E10
16	PB7	GPIO 30	A10
17	PC0	GPIO 84	D16
18	PC1	GPIO 83	E15
19	PC2	GPIO 81	F16
20	PC3	GPIO 82	E16

Table 4-5: DNP/2110 PIO pin mapping to PXA255 pins

4.8 Memory Mapping

Function Unit	Startaddress	Endaddress	Access Format
16MBytes Flash	0x0000.0000	0x03FF.FFFF	16 Bits
Ethernet LAN Controller	0x0400.0000	0x07FF.FFFF	32 Bits
CS1_Space	0x3000.0000	0x30FF.FFFF	8 Bits
CS2_Space	0x3100.0000	0x31FF.FFFF	8 Bits
CS3_Space	0x3200.0000	0x32FF.FFFF	8 Bits
CS4_Space	0x3300.0000	0x33FF.FFFF	8 Bits
PXA255 Internal Registers	0x4000.0000	0x4BFF.FFFF	32 Bits
16Mbytes SDRAM	0xA000.0000	0xA3FF.FFFF	32 Bits

Table 4-6: DNP/2110 memory mapping (physical addresses)

The four memory areas called *CS1_Space* to *CS4_Space* are reserved for the four chip select output pins CS1, CS2, CS3 and CS4 of the DNP/2110.

User programs are located from default start address 0xA020:0000 within the DNP/2110 memory space.

4.9 Bus Signal Mapping (8-bit I/O Expansion Bus)

The 27 pins of the DNP/2110 8-bit I/O Expansion Bus are directly connected to signals of the Intel PXA255 Xscale 32-bit microcontroller. The following table shows this mapping.

Pin	Name	PXA255 Pin Function	PXA255 Pin
29	RESIN	Supervisor	---
35	RESOUT	nRESET_OUT	K11
37	CLKOUT	3.6MHz	A7
40	INT5	GPIO 22 (IS10)	M12
41	INT4	GPIO 21 (IS10)	N15
42	INT3	GPIO 20 (IS10)	N12
43	INT2	GPIO 19 (IS10)	N14
44	INT1	GPIO 1 (IS9)	L12
45	CS4	---	---
46	CS3	---	---
47	CS2	---	---
48	CS1	---	---
49	IOCHRDY	nPWAIT	N16
50	IOR	nPIOR	T15
51	IOW	nPIOW	R15
52	SA3	MA3	H6
53	SA2	MA2	H1
54	SA1	MA1	H2
55	SA0	MA0	G1
56	SD7	MD7	M6
57	SD6	MD6	M7
58	SD5	MD5	T7
59	SD4	MD4	N6
60	SD3	MD3	T6
61	SD2	MD2	L5
62	SD1	MD1	M5
63	SD0	MD0	N4

Table 4-7: DNP/2110 expansion bus pin mapping to PXA255 pins

Please see also the *Intel PXA255 Processor Developer's Manual* and the *Intel PXA255 Processor Data Sheet* for the PXA255 pin function details.

The chip select output pins CS1, CS2, CS3 and CS4 are driven by a 74AHC138 address decoder chip.

4.10 Connecting an External Battery

To ensure the external RTC (Real Time Clock) function of the DNP/2110 when the main power is removed a backup battery must be connected between VBAT (pin 36) and GND. If main power is turned on – no battery power will be consumed.

The backup battery should be a lithium battery with a voltage of approx. 3V DC. We recommend a Renata battery, type CR2032 with 3.3V and 150mAh.

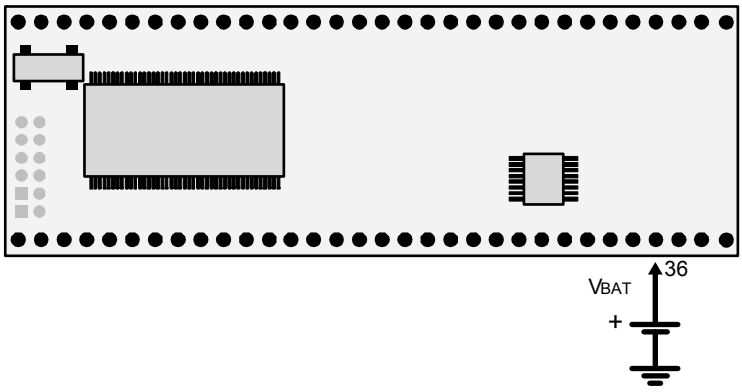


Figure 4-2: Connecting an external battery to pin 36 of the DNP/2110

CONTACT

SSV Embedded Systems
Heisterbergallee 72
D-30453 Hannover
Phone +49-(0)511-40000-0
Fax +49-(0)511-40000-40
E-mail: sales@ist1.de
Internet: www.ssv-embedded.de

DOCUMENT HISTORY

Revision	Date	Remarks	Name
1.0	2004-09-10	first version	WBU

This document is written only for the internal application. The content of this document can change any time without announcement. There is taken over no guarantee for the accuracy of the statements.