CP/486SX2-SV4

Board Revision 1.1b

Hardware Reference

SSV Embedded Systems
Heisterbergallee 72
D-30453 Hannover
Phone: +49-(0)511-40000-0
Fax: +49-(0)511-40000-40
E-mail: sales@ist1.de

Manual Revision: 1.1
Date: 2006-01-24

For further information regarding our products please visit us at www.dilnetpc.com

CONTENT

1 INTRODUCTION

This document describes the hardware components of the DIL/NetPC application board CP/486SX2-SV4. For further information about the individual components of this product you may follow the links from the website http://www.dilnetpc.com. This website contains a lot of technical information, which will be updated in regular periods. Figure 1 shows the block diagram of the CP/486SX2-SV4.

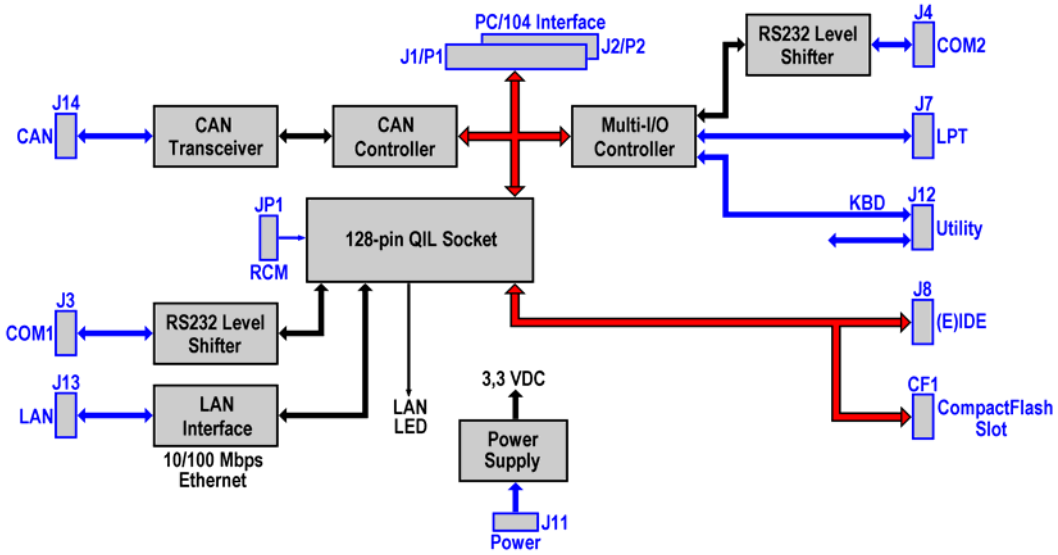


Figure 1: Block diagram of DIL/NetPC application board CP/486SX2-SV4

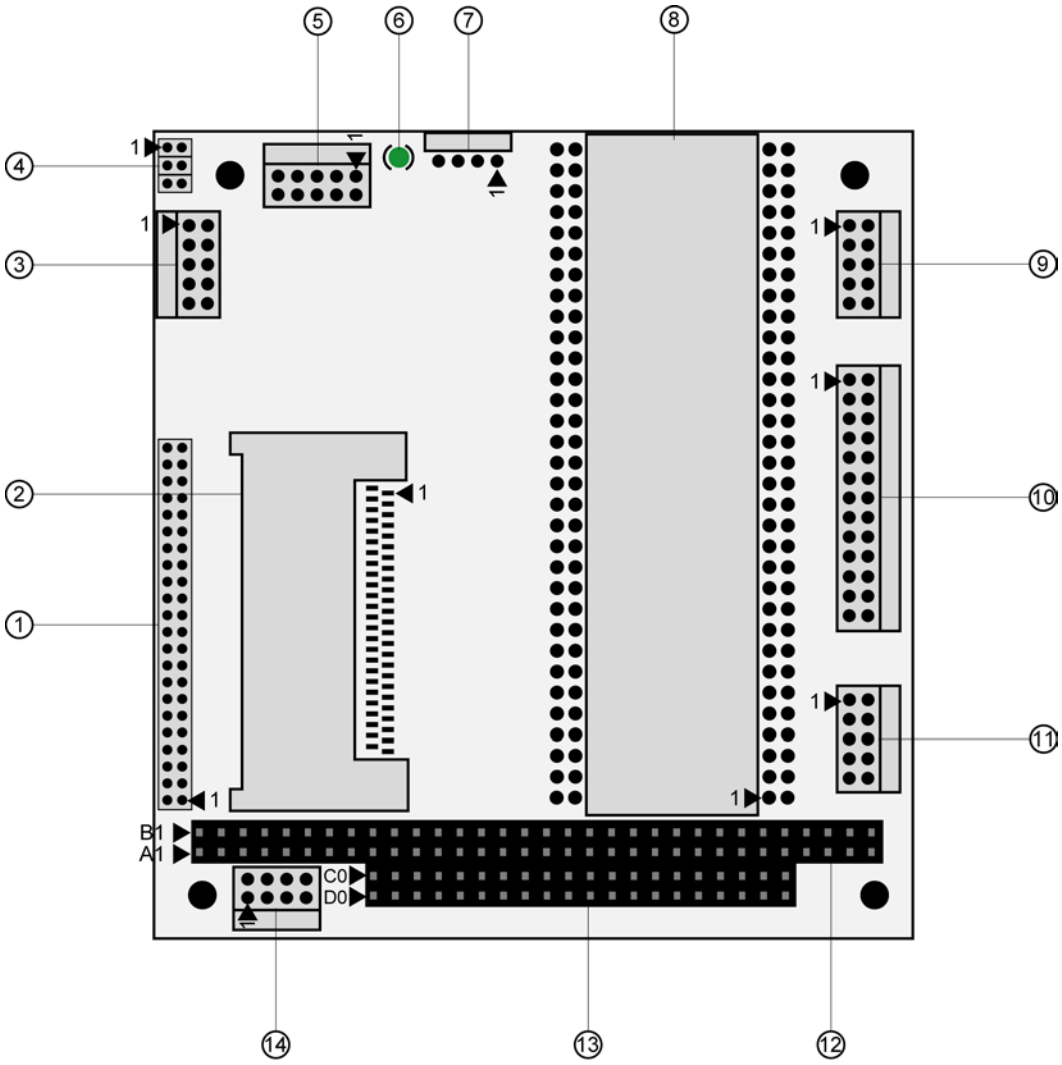
The DIL/NetPC application board CP/486SX2-SV4 provides in the center one QIL-128 pin socket for the ADNP/1520. The CP/486SX2-SV4 includes the external parts for the ADNP/1520 COM1 serial port and the 10/100 Mbps Ethernet LAN interface. There is also a CompactFlash (CF) slot available for using the ADNP/1520 with CompactFlash memory cards. Instead of CF, it is also possible to use external hard disk drives with 44-pin IDE connectors (i.e. 2.5" notebook drives). The CP/486SX2-SV4 expands the ADNP/1520 with one SJA1000 CAN controller and one Multi-I/O controller chip.

The CP/486SX2-SV4 uses the PC/104 form factor with 90 x 96 mm and the PC/104 connectors J1/P1, J2/P2 for expansion.

1.1 Features CP/486SX2-SV4

- Two RS232 serial ports (COM1 and COM2)
- One parallel port with SPP-, EPP-, ECP- modes
- One 4-pin 10/100 Mbps Ethernet interface
- One green LAN activity LED
- One CompactFlash slot
- Optional Enhanced IDE interface for two devices
- One standard 16-bit PC/104 interface
- One Speaker port, 0.1 Watt drive
- One SJA1000 CAN controller with interface circuit
- Jumper for Remote Console Mode (RCM)
- Size 90 x 96 mm (standard PC/104 form factor)
- Supply voltage 5 VDC (±5 %)
- Operating temperature 0° to +60° C
- Storage temperature -55° to +85° C
- Relative humidity 10 % to 90 %, non condensing
- Power consumption 5,5W max. by use of ADNP/1520 at 133 MHz

2 BOARD LAYOUT



① J8 - (E)IDE connector
② CF1 - CompactFlash slot
③ J4 - COM2 connector
④ JP1 - Configuration jumper
⑤ J14 - CAN connector
⑥ LAN activity LED
⑦ J13 -10/100 Mbps Ethernet connector
⑧ 128-pin QIL socket
⑨ J3 - COM1 connector
⑩ J7 - LPT connector
⑪ J12 - Utility connector
⑫ J1/P1 - PC-104 64-pin interface
⑬ J2/P2 - PC-104 40-pin interface
⑭ J11 - Power connector

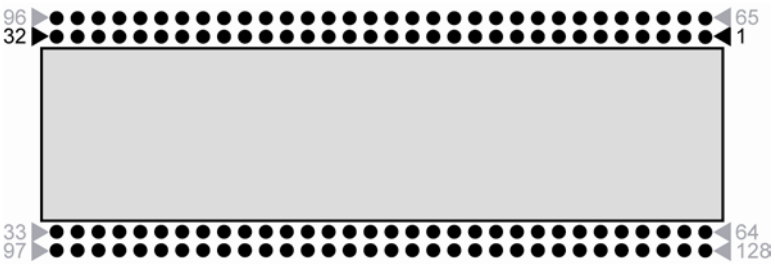
Figure 2: Board layout CP/486SX2-SV4

3 PINOUTS

3.1 128-pin QIL Socket (1. Part)

Pin	Name	Group	Function
1	PA0	PIO	Parallel I/O, Port A, Bit 0
2	PA1	PIO	Parallel I/O, Port A, Bit 1
3	PA2	PIO	Parallel I/O, Port A, Bit 2
4	PA3	PIO	Parallel I/O, Port A, Bit 3
5	PA4	PIO	Parallel I/O, Port A, Bit 4
6	PA5	PIO	Parallel I/O, Port A, Bit 5
7	PA6	PIO	Parallel I/O, Port A, Bit 6
8	PA7	PIO	Parallel I/O, Port A, Bit 7
9	PB0	PIO	Parallel I/O, Port B, Bit 0
10	PB1	PIO	Parallel I/O, Port B, Bit 1
11	PB2	PIO	Parallel I/O, Port B, Bit 2
12	PB3	PIO	Parallel I/O, Port B, Bit 3
13	PB4	PIO	Parallel I/O, Port B, Bit 4
14	PB5	PIO	Parallel I/O, Port B, Bit 5
15	PB6	PIO	Parallel I/O, Port B, Bit 6
16	PB7	PIO	Parallel I/O, Port B, Bit 7
17	PC0	PIO	Parallel I/O, Port C, Bit 0
18	PC1	PIO	Parallel I/O, Port C, Bit 1
19	PC2	PIO	Parallel I/O, Port C, Bit 2
20	PC3	PIO	Parallel I/O, Port C, Bit 3
21	RXD1	SIO	COM1 Serial Port, RXD Pin
22	TXD1	SIO	COM1 Serial Port, TXD Pin
23	CTS1	SIO	COM1 Serial Port, CTS Pin
24	RTS1	SIO	COM1 Serial Port, RTS Pin
25	DCD1	SIO	COM1 Serial Port, DCD Pin
26	DSR1	SIO	COM1 Serial Port, DSR Pin
27	DTR1	SIO	COM1 Serial Port, DTR Pin
28	RI1	SIO	COM1 Serial Port, RI Pin
29	RESIN	RESET	RESET Input
30	TX+	LAN	10/100 Mbps Ethernet Interface, TX+ Pin
31	TX-	LAN	10/100 Mbps Ethernet Interface, TX- Pin
32	GND	---	Ground

Table 1: 128-pin QIL socket pinout – pin 1 to 32

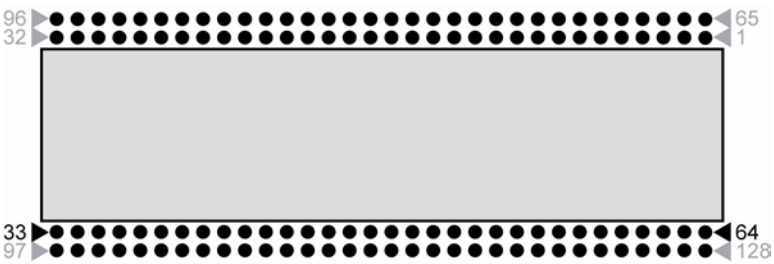


3.2 128-pin QIL Socket (2. Part)

Pin	Name	Group	Function
33	RX+	LAN	10/100 Mbps Ethernet Interface, RX+ Pin
34	RX-	LAN	10/100 Mbps Ethernet Interface, RX- Pin
35	RESOUT	RESET	RESET Output
36	VBAT	PSP*	Real Time Clock Battery Input
37	CLKOUT	PSP*	Clock Output
38	TXD2	PSP*	COM2 Serial Port, TXD Pin
39	RXD2	PSP*	COM2 Serial Port, RXD Pin
40	INT5	PSP*	Programmable Interrupt Input 5
41	INT4	PSP*	Programmable Interrupt Input 4
42	INT3	PSP*	Programmable Interrupt Input 3
43	INT2	PSP*	Programmable Interrupt Input 2
44	INT1	PSP*	Programmable Interrupt Input 1
45	CS4	PSP*	Programmable Chip Select Output 4
46	CS3	PSP*	Programmable Chip Select Output 3
47	CS2	PSP*	Programmable Chip Select Output 2
48	CS1	PSP*	Programmable Chip Select Output 1
49	IOCHRDY	PSP*	I/O Channel Ready
50	IOR	PSP*	I/O Read Signal, I/O Expansion Bus
51	IOW	PSP*	I/O Write Signal, I/O Expansion Bus
52	SA3	PSP*	System Expansion Bus, Address Bit 3
53	SA2	PSP*	System Expansion Bus, Address Bit 2
54	SA1	PSP*	System Expansion Bus, Address Bit 1
55	SA0	PSP*	System Expansion Bus, Address Bit 0
56	SD7	PSP*	System Expansion Bus, Data Bit 7
57	SD6	PSP*	System Expansion Bus, Data Bit 6
58	SD5	PSP*	System Expansion Bus, Data Bit 5
59	SD4	PSP*	System Expansion Bus, Data Bit 4
60	SD3	PSP*	System Expansion Bus, Data Bit 3
61	SD2	PSP*	System Expansion Bus, Data Bit 2
62	SD1	PSP*	System Expansion Bus, Data Bit 1
63	SD0	PSP*	System Expansion Bus, Data Bit 0
64	Vcc	---	3.3 Volt Power Input

* = Product Specific Pins

Table 2: 128-pin QIL socket pinout – pin 33 to 64

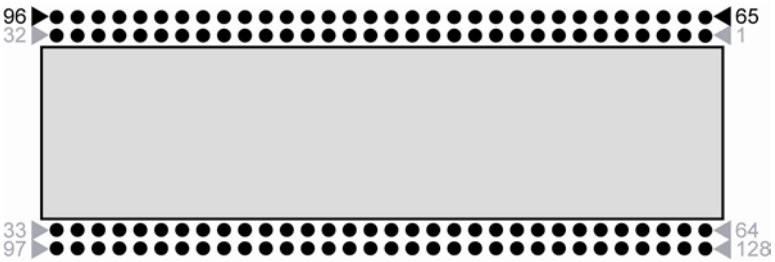


3.3 128-pin QIL Socket (3. Part)

Pin	Name	Group	Function
65	SBHE	PSP*	System Byte High Enable, System Expansion Bus
66	IOCS16	PSP*	I/O Chip Select 16, System Expansion Bus
67	Reserved	PSP*	Reserved
68	Reserved	PSP*	Reserved
69	Reserved	PSP*	Reserved
70	BALE	PSP*	Bus Latch Enable, System Expansion Bus
71	AEN	PSP*	Address Enable Signal, System Expansion Bus
72	Reserved	PSP*	Reserved – Do not use
73	RCME	PSP*	Remote Console Mode Enable
74	Reserved	PSP*	Reserved – Do not use
75	Reserved	PSP*	Reserved – Do not use
76	Reserved	PSP*	Reserved – Do not use
77	Reserved	PSP*	Reserved – Do not use
78	Reserved	PSP*	Reserved – Do not use
79	Reserved	PSP*	Reserved – Do not use
80	Reserved	PSP*	Reserved – Do not use
81	Reserved	PSP*	Reserved – Do not use
82	Reserved	PSP*	Reserved – Do not use
83	Reserved	PSP*	Reserved – Do not use
84	Reserved	PSP*	Reserved – Do not use
85	INT6	PSP*	Programmable Interrupt Input 6
86	INT7	PSP*	Programmable Interrupt Input 7
87	IDERES	PSP*	IDE Interface Reset Output
88	IDECS0	PSP*	IDE Interface Chip Select 0
89	IDECS1	PSP*	IDE Interface Chip Select 1
90	Reserved	PSP*	Reserved – Do not use
91	Reserved	PSP*	Reserved – Do not use
92	Reserved	PSP*	Reserved – Do not use
93	Reserved	PSP*	Reserved – Do not use
94	Reserved	PSP*	Reserved – Do not use
95	Reserved	PSP*	Reserved – Do not use
96	GND	---	Ground

* = Product Specific Pins

Table 3: 128-pin QIL socket pinout – pin 65 to 96

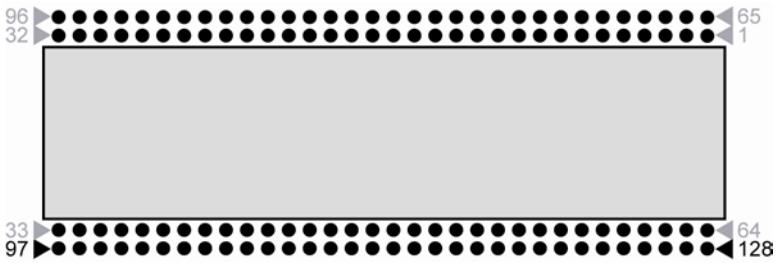


3.4 128-pin QIL Socket (4. Part)

Pin	Name	Group	Function
97	LANLED	PSP*	LAN Interface Activty LED
98	Reserved	PSP*	Reserved – Do not use
99	RSTDRV	PSP*	Reset Output, System Expansion Bus
100	SA23	PSP*	System Expansion Bus, Address Bit 23
101	SA22	PSP*	System Expansion Bus, Address Bit 22
102	SA21	PSP*	System Expansion Bus, Address Bit 21
103	SA20	PSP*	System Expansion Bus, Address Bit 20
104	SA19	PSP*	System Expansion Bus, Address Bit 19
105	SA18	PSP*	System Expansion Bus, Address Bit 18
106	SA17	PSP*	System Expansion Bus, Address Bit 17
107	SA16	PSP*	System Expansion Bus, Address Bit 16
108	SA15	PSP*	System Expansion Bus, Address Bit 15
109	SA14	PSP*	System Expansion Bus, Address Bit 14
110	SA13	PSP*	System Expansion Bus, Address Bit 13
111	SA12	PSP*	System Expansion Bus, Address Bit 12
112	SA11	PSP*	System Expansion Bus, Address Bit 11
113	SA10	PSP*	System Expansion Bus, Address Bit 10
114	SA9	PSP*	System Expansion Bus, Address Bit 9
115	SA8	PSP*	System Expansion Bus, Address Bit 8
116	SA7	PSP*	System Expansion Bus, Address Bit 7
117	SA6	PSP*	System Expansion Bus, Address Bit 6
118	SA5	PSP*	System Expansion Bus, Address Bit 5
119	SA4	PSP*	System Expansion Bus, Address Bit 4
120	SD15	PSP*	System Expansion Bus, Data Bit 15
121	SD14	PSP*	System Expansion Bus, Data Bit 14
122	SD13	PSP*	System Expansion Bus, Data Bit 13
123	SD12	PSP*	System Expansion Bus, Data Bit 12
124	SD11	PSP*	System Expansion Bus, Data Bit 11
125	SD10	PSP*	System Expansion Bus, Data Bit 10
126	SD9	PSP*	System Expansion Bus, Data Bit 9
127	SD8	PSP*	System Expansion Bus, Data Bit 8
128	Vcc	---	3.3 Volt Power Input

* = Product Specific Pins

Table 4: 128-pin QIL socket pinout – pin 97 to 128



3.5 PC/104 64-pin Interface – J1/P1 (1. Part)

The J1/P1 interface forms the 8-bit PC/104 bus. The extension onto a 16-bit PC/104 bus occurs by the J2/P2 interface (please refer to **chapter 3.7**).

Pin	Name	Function	In/Out
A1	IOCHK#	Bus NMI Input	IN
A2	SD7	Data Bit 7	I/O
A3	SD6	Data Bit 6	I/O
A4	SD5	Data Bit 5	I/O
A5	SD4	Data Bit 4	I/O
A6	SD3	Data Bit 3	I/O
A7	SD2	Data Bit 2	I/O
A8	SD1	Data Bit 1	I/O
A9	SD0	Data Bit 0	I/O
A10	IOCHRDY	Processor Ready Ctrl	IN
A11	AEN	Address Enable	I/O
A12	SA19	Address Bit 19	I/O
A13	SA18	Address Bit 18	I/O
A14	SA17	Address Bit 17	I/O
A15	SA16	Address Bit 16	I/O
A16	SA15	Address Bit 15	I/O
A17	SA14	Address Bit 14	I/O
A18	SA13	Address Bit 13	I/O
A19	SA12	Address Bit 12	I/O
A20	SA11	Address Bit 11	I/O
A21	SA10	Address Bit 10	I/O
A22	SA9	Address Bit 9	I/O
A23	SA8	Address Bit 8	I/O
A24	SA7	Address Bit 7	I/O
A25	SA6	Address Bit 6	I/O
A26	SA5	Address Bit 5	I/O
A27	SA4	Address Bit 4	I/O
A28	SA3	Address Bit 3	I/O
A29	SA2	Address Bit 2	I/O
A30	SA1	Address Bit 1	I/O
A31	SA0	Address Bit 0	I/O
A32	GND	Ground	N/A

Table 5: PC/104 64-pin interface pinout - pin A1 to A32

3.6 PC/104 64-pin Interface – J1/P1 (2. Part)

Pin	Name	Function	In/Out
B1	GND	Ground	N/A
B2	RESETDRV	System Reset Signal	OUT
B3	+5 VDC	+5 Volt Power	N/A
B4	IRQ9	Interrupt Request 9	IN
B5	-5 VDC	-5 Volt Power	N/A
B6	DRQ2	DMA Request 2	IN
B7	-12 VDC	-12 Volt Power	N/A
B8	ENDXFR#	Zero Wait State	IN
B9	+12 VDC	+12 Volt Power	N/A
B10	---	Not Connected	N/A
B11	SMEMW#	Memory Write (first MB)	I/O
B12	SMEMR#	Memory Read (first MB)	I/O
B13	IOW#	I/O Write	I/O
B14	IOR#	I/O Read	I/O
B15	DACK3#	DMA Acknowledge 3	OUT
B16	DRQ3	DMA Request 3	IN
B17	DACK1#	DMA Acknowledge 1	OUT
B18	DRQ1	DMA Request 1	IN
B19	REFRESH#	Memory Refresh	I/O
B20	SYSCLK	System Clock (e.g. 8 MHz)	OUT
B21	IRQ7	Interrupt Request 7	IN
B22	IRQ6	Interrupt Request 6	IN
B23	IRQ5	Interrupt Request 5	IN
B24	IRQ4	Interrupt Request 4	IN
B25	IRQ3	Interrupt Request 3	IN
B26	DACK2#	DMA Acknowledge 2	OUT
B27	TC	DMA Terminal Count	OUT
B28	BALE	Address Latch Enable	OUT
B29	+5 VDC	+5 Volt Power	N/A
B30	OSC	14.3 MHz Clock	OUT
B31	GND	Ground	N/A
B32	GND	Ground	N/A

Table 6: PC/104 64-pin interface pinout – pin B1 to B32

3.7 PC/104 40-pin Interface – J2/P2

The J2/P2 interface forms the 16-bit PC/104 bus.

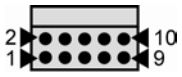
Pin	Name	Function	In/Out
C0	GND	Ground	N/A
C1	SBHE#	Bus High Enable	I/O
C2	LA23	Address Bit 23	I/O
C3	LA22	Address Bit 22	I/O
C4	LA21	Address Bit 21	I/O
C5	LA20	Address Bit 20	I/O
C6	LA19	Address Bit 19	I/O
C7	LA18	Address Bit 18	I/O
C8	LA17	Address Bit 17	I/O
C9	MEMR#	Memory Read	I/O
C10	MEMW#	Memory Write	I/O
C11	SD8	Data Bit 8	I/O
C12	SD9	Data Bit 9	I/O
C13	SD10	Data Bit 10	I/O
C14	SD11	Data Bit 11	I/O
C15	SD12	Data Bit 12	I/O
C16	SD13	Data Bit 13	I/O
C17	SD14	Data Bit 14	I/O
C18	SD15	Data Bit 15	I/O
C19	GND	Ground	N/A
D0	GND	Ground	N/A
D1	MEMCS16#	16 -Bit Memory Access	IN
D2	IOCS16#	16-Bit I/O Access	IN
D3	IRQ10	Interrupt Request 10	IN
D4	IRQ11	Interrupt Request 11	IN
D5	IRQ12	Interrupt Request 12	IN
D6	IRQ15	Interrupt Request 15	IN
D7	IRQ14	Interrupt Request 14	IN
D8	DACK0#	DMA Acknowledge 0	OUT
D9	DRQ0	DMA Request 0	IN
D10	DACK5#	DMA Acknowledge 5	OUT
D11	DRQ5	DMA Request 5	IN
D12	DACK6#	DMA Acknowledge 6	OUT
D13	DRQ6	DMA Request 6	IN
D14	DACK7#	DMA Acknowledge 7	OUT
D15	DRQ7	DMA Request 7	IN
D16	+5 VDC	+5 Volt Power	N/A
D17	MASTER#	Bus Master Assert	IN
D18	GND	Ground	N/A
D19	GND	Ground	N/A

Table 7: PC/104 40-pin interface pinout

3.8 COM1 Connector – J3

Pin	Name	Function	In/Out
1	DCD	Data Carrier Detect	IN
2	DSR	Data Set Ready	IN
3	RXD	Receive Data	IN
4	RTS	Request To Send	OUT
5	TXD	Transmit Data	OUT
6	CTS	Clear To Send	IN
7	DTR	Data Terminal Ready	OUT
8	RI	Ring Indicator	IN
9	GND	Ground	N/A
10	---	Not Connected	N/A

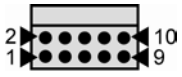
Table 8: Pinout COM1 connector



3.9 COM2 Connector – J4

Pin	Name	Function	In/Out
1	DCD	Data Carrier Detect	IN
2	DSR	Data Set Ready	IN
3	RXD	Receive Data	IN
4	RTS	Request To Send	OUT
5	TXD	Transmit Data	OUT
6	CTS	Clear To Send	IN
7	DTR	Data Terminal Ready	OUT
8	RI	Ring Indicator	IN
9	GND	Ground	N/A
10	---	Not Connected	N/A

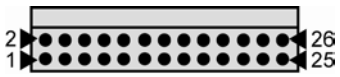
Table 9: Pinout COM2 connector



3.10 LPT Connector – J7

Pin	Name	Function	In/Out
1	STRB#	Output Data Strobe	OUT
2	AUTOFD#	Autofeed	OUT
3	PD0	Printer Data Bit 0 (LSB)	I/O
4	ERROR#	Printer Error	IN
5	PD1	Printer Data Bit 1	I/O
6	INIT#	Initialize Printer	OUT
7	PD2	Printer Data Bit 2	I/O
8	SLCTIN	Select Printer	OUT
9	PD3	Printer Data Bit 3	I/O
10	GND	Ground	N/A
11	PD4	Printer Data Bit 4	I/O
12	GND	Ground	N/A
13	PD5	Printer Data Bit 5	I/O
14	GND	Ground	N/A
15	PD6	Printer Data Bit 6	I/O
16	GND	Ground	N/A
17	PD7	Printer Data Bit 7 (MSB)	I/O
18	GND	Ground	N/A
19	ACK#	Character Accepted	IN
20	GND	Ground	N/A
21	BUSY	Cannot Receive Data	IN
22	GND	Ground	N/A
23	PE	Paper Empty	IN
24	GND	Ground	N/A
25	SLCTOUT	Printer Selected	IN
26	---	Not Connected	N/A

Table 10: Pinout LPT connector



3.11 (E)IDE Connector – J8 (1. Part)

Pin	Name	Function	In/Out
1	RESET#	Device Reset	OUT
2	GND	Ground	N/A
3	DD7	Drive Data Bit 7	I/O
4	DD8	Drive Data Bit 8	I/O
5	DD6	Drive Data Bit 6	I/O
6	DD9	Drive Data Bit 9	I/O
7	DD5	Drive Data Bit 5	I/O
8	DD10	Drive Data Bit 10	I/O
9	DD4	Drive Data Bit 4	I/O
10	DD11	Drive Data Bit 11	I/O
11	DD3	Drive Data Bit 3	I/O
12	DD12	Drive Data Bit 12	I/O
13	DD2	Drive Data Bit 2	I/O
14	DD13	Drive Data Bit 13	I/O
15	DD1	Drive Data Bit 1	I/O
16	DD14	Drive Data Bit 14	I/O
17	DD0	Drive Data Bit 0	I/O
18	DD15	Drive Data Bit 15	I/O
19	GND	Ground	N/A
20	---	Not Connected	N/A
21	---	Not Connected	N/A
22	GND	Ground	N/A

Table 11: Pinout (E)IDE connector part 1

3.12 (E)IDE Connector – J8 (2. Part)

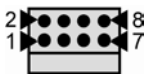
Pin	Name	Function	In/Out
23	DIOW#	Drive I/O Write	OUT
24	GND	Ground	N/A
25	DIOR#	Drive I/O Read	OUT
26	GND	Ground	N/A
27	IORDY	I/O Channel Ready	IN
28	---	Not Connected	N/A
29	---	Not Connected	N/A
30	GND	Ground	N/A
31	INTRQ	Drive Interrupt Req.	IN
32	IOCS16#	Drive 16 Bit I/O	IN
33	DA1	Drive Address Bit 1	OUT
34	---	Not Connected	N/A
35	DA0	Drive Address Bit 0	OUT
36	DA2	Drive Address Bit 2	OUT
37	CS0#	Chip Select Drive 0	OUT
38	CS1#	Chip Select Drive 1	OUT
39	DACT#	Drive Active	IN
40	GND	Ground	N/A
41	+5 VDC	+5 Volt Power	N/A
42	+5 VDC	+5 Volt Power	N/A
43	GND	Ground	N/A
44	---	Not Connected	N/A

Table 12: Pinout (E)IDE connector part 2

3.13 Power Connector – J11

Pin	Name	Function	In/Out
1	GND	Ground	N/A
2	+5 VDC	+5 Volt Power Input	N/A
3	---	Not Connected	N/A
4	---	Not Connected	N/A
5	---	Not Connected	N/A
6	---	Not Connected	N/A
7	GND	Ground	N/A
8	+5 VDC	+5 Volt Power Input	N/A

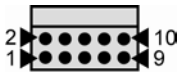
Table 13: Pinout power connector



3.14 Utility Connector – J12

Pin	Name	Function	In/Out
1	EXTSPK	External Speaker	OUT
2	GND	Ground	N/A
3	EXTRST	External Reset Input	IN
4	KBLOCK#	Keyboard Lock	IN
5	KBDDAT	Keyboard Data	I/O
6	KBDCLK	Keyboard Clock	I/O
7	GND	Ground	N/A
8	KBDVCC	Keyboard +5 Volt Power	N/A
9	EXTBAT	External Battery Power Input	N/A
10	PWRGD	Power Good	IN

Table 14: Pinout utility connector



3.15 10/100 Mbps Ethernet Connector – J13

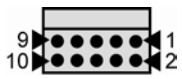
Pin	Name	Function	In/Out
1	TX+	Transmit Data Plus	OUT
2	TX-	Transmit Data Minus	OUT
3	RX+	Receive Data Plus	IN
4	RX-	Receive Data Minus	IN

Table 15: Pinout 10/100 Mbps Ethernet connector

3.16 CAN Connector – J14

Pin	Name	Function	In/Out
1	---	Not Connected	N/A
2	GND	Signal Ground	N/A
3	CAN-L	Signal LOW	N/A
4	CAN-H	Signal HIGH	N/A
5	GND	Signal Ground	N/A
6	---	Not Connected	N/A
7	---	Not Connected	N/A
8	---	Not Connected	N/A
9	---	Not Connected	N/A
10	---	Not Connected	N/A

Table 16: Pinout CAN connector



3.17 CompactFlash Slot – CF1 (1. Part)

Pin	Name	Function	In/Out
1	GND	Ground	N/A
2	D3	SD3	N/A
3	D4	SD4	N/A
4	D5	SD5	N/A
5	D6	SD6	N/A
6	D7	SD7	N/A
7	CS0#	IDE_4	N/A
8	A10	Ground	N/A
9	ATASEL#	Ground	N/A
10	A9	Ground	N/A
11	A8	Ground	N/A
12	A7	Ground	N/A
13	Vcc	Power	N/A
14	A6	Ground	N/A
15	A5	Ground	N/A
16	A4	Ground	N/A
17	A3	Ground	N/A
18	A2	SA2/4*	N/A
19	A1	SA1/3*	N/A
20	A0	SA0/2*	N/A
21	D0	SD0	N/A
22	D1	SD1	N/A
23	D2	SD2	N/A
24	IOCS16#	IDE_7	N/A
25	CD2#	---	N/A

Table 17: Pinout CompactFlash slot – pin 1 to 25

Note: The CompactFlash slot works only with CF cards in True IDE mode. The CF cards must be hardwired as master.

3.18 CompactFlash Slot – CF1 (2. Part)

Pin	Name	Function	In/Out
26	CD1#	---	N/A
27	D11	SD11	N/A
28	D12	SD12	N/A
29	D13	SD13	N/A
30	D14	SD14	N/A
31	D15	SD15	N/A
32	CS1#	IDE_3	N/A
33	VS1#	---	N/A
34	IOR#	IDE_1	N/A
35	IOW#	IDE_0	N/A
36	WE#	Vcc3	N/A
37	IRQ	IDE_6	N/A
38	Vcc	Power	N/A
39	CSEL#	IDE_10	N/A
40	VS2	---	N/A
41	RESET#	IDE_5	N/A
42	IOCHRDY#	IDE_2	N/A
43	INPACK#	---	N/A
44	REG#	Vcc3	N/A
45	DASP#	IDE_9	N/A
46	PDIAG#	IDE_8	N/A
47	D8	SD8	N/A
48	D9	SD9	N/A
49	D10	SD10	N/A
50	GND	Ground	N/A

Table 18: Pinout CompactFlash slot – pin 26 to 50

Note: The CompactFlash slot works only with CF cards in True IDE mode. The CF cards must be hardwired as master.

3.19 Configuration Jumper – JP1

The CP/486SX2-SV4 is equipped with a 6-pin jumper field to use for system-setup settings. By that you are able to activate or deactivate the Remote Console Mode and/or the Flash BIOS Hardware Lock.

Jumper Position	Status	Function
Pin 1 – 2	open	reserved
Pin 1 – 2	closed	reserved
Pin 3 – 4	open	Remote Console Mode (RCM) deactivated
Pin 3 – 4	closed	Remote Console Mode (RCM) activated
Pin 5 – 6	open	Flash BIOS Hardware Lock activated
Pin 5 – 6	closed	Flash BIOS Hardware Lock deactivated

Table 19: Jumper settings

4 MECHANICAL DIMENSIONS

All length dimensions have a tolerance of 0.5 mm.

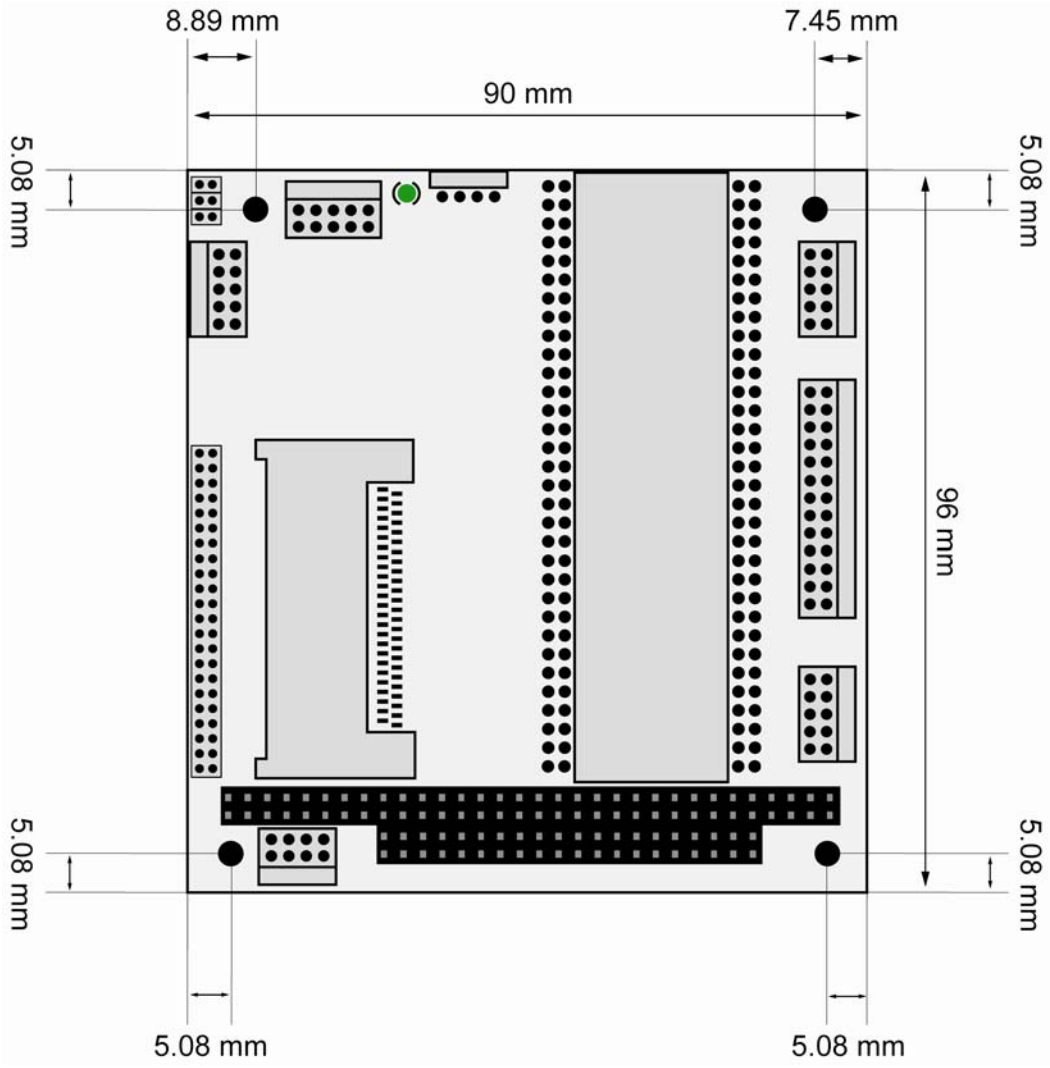


Figure 3: Mechanical dimensions of CP/486SX2-SV4

The drillings are suitable for M3 screws.

CONTACT

SSV Embedded Systems
Heisterbergallee 72
D-30453 Hannover
Phone: +49-(0)511-40000-0
Fax: +49-(0)511-40000-40
E-mail: sales@ist1.de
Internet: www.dilnetpc.com

DOCUMENT HISTORY

Revision	Date	Remarks	Name
1.0	2005-05-23	first version	WBU
1.1	2006-01-24	New cover foto (ADNP/1520 position)	WBU

The content of this document can change any time without announcement. There is taken over no guarantee for the accuracy of the statements. The user assumes the entire risk as to the accuracy and the use of this document. Information in this document is provided 'as is' without warranty of any kind.

Some names within this document can be trademarks of their respective holders.