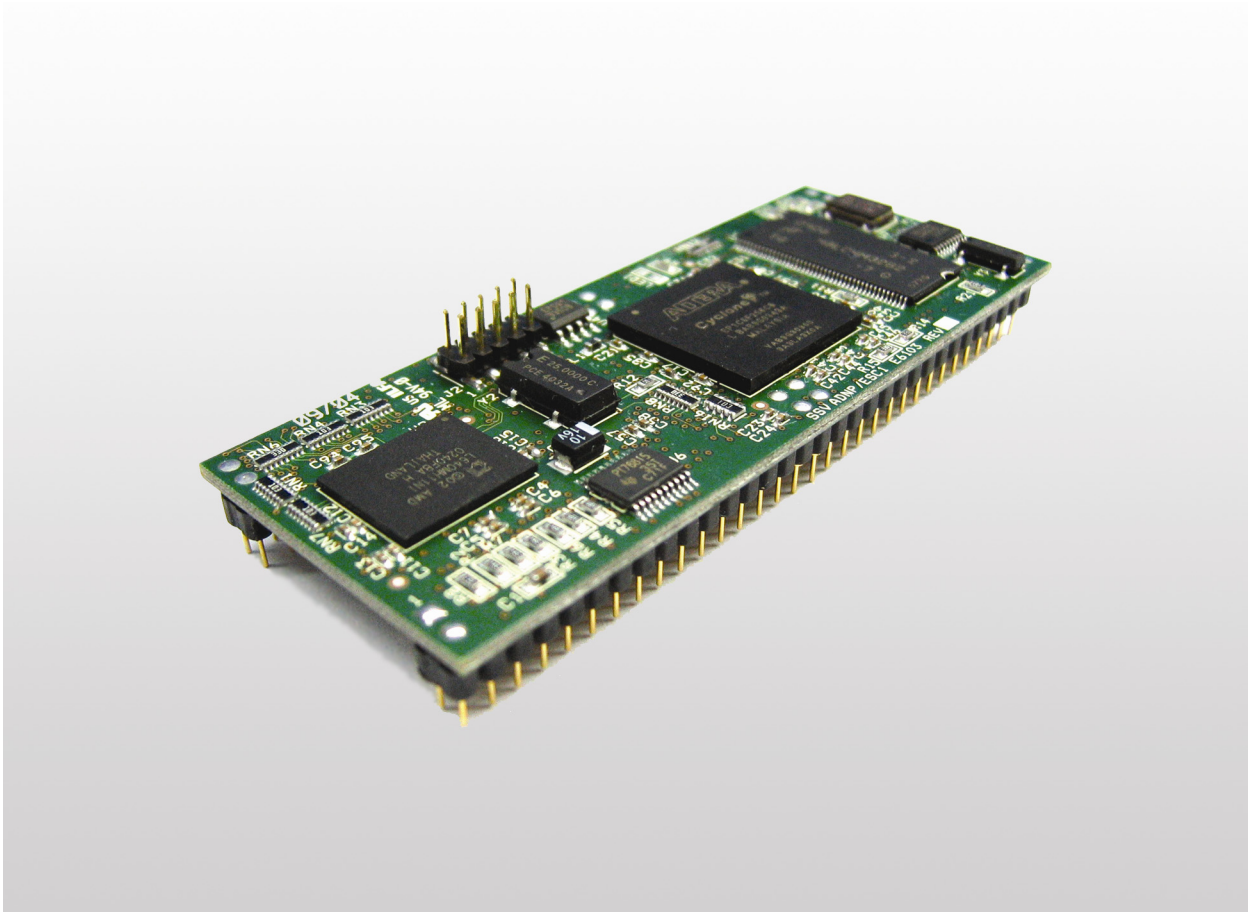
DIL/NetPC ADNP/ESC1
Revision 1.0

Hardware Reference



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For further information regarding our products please visit us at www.dilnetpc.com

CONTENT

1 INTRODUCTION

This document describes the components of the ADNP/ESC1. For further information about this product you may follow the links from our website at *http://www.dilnetpc.com.*

Our Website contains a lot of technical information, which will be updated in regular periods.

1.1 Block Diagram

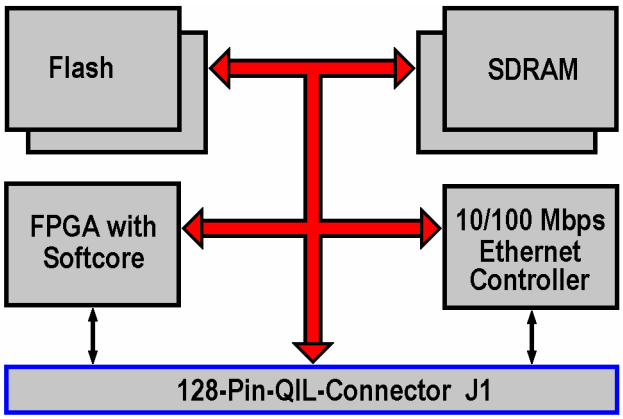
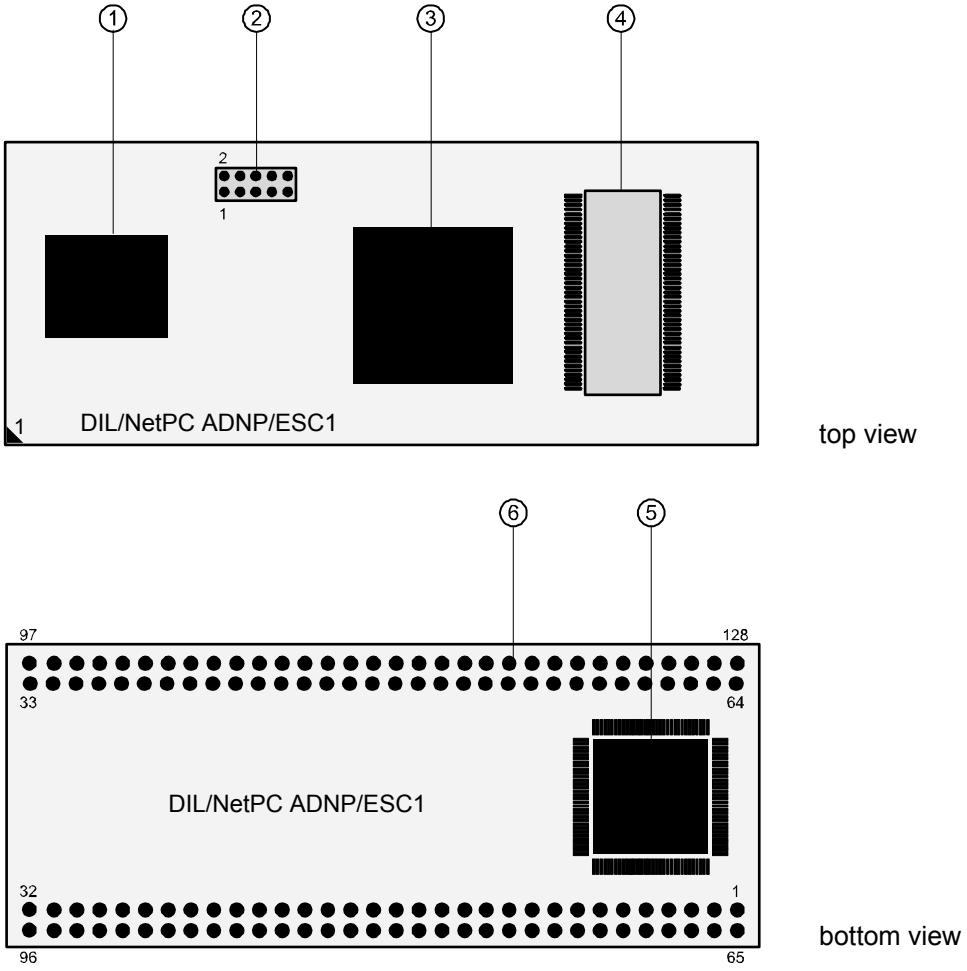


Figure 1-1: ADNP/ESC1 block diagram

1.2 Features DIL/NetPC ADNP/ESC1

- Altera 32-bit NIOS RISC Softcore with 512 internal Registers
- 50 MHz Operation
- 16 MByte SDRAM Memory with 32-bit Data Path
- 8 MByte Flash Memory with 16-bit Data Path
- 10/100 Mbps Ethernet LAN Interface
- Two asynchronous Serial Ports (one with Handshakes)
- 20-bit General Purpose high-speed Parallel I/O
- 16-bit ISA-like Expansion Bus
- IDE Interface with CompactFlash Support (True IDE Mode)
- Seven Interrupt Inputs
- Four Chip Select Outputs
- Programmable General Purpose Timers and Watchdog Timer
- JTAG IEEE 1149.1 Test Interface
- In-System Programming Features
- 128-pin QIL (Quad-In-Line) Connector, 2.54mm Centers
- 3.3 Volt Low Power Design, Supply Voltage 3.3 VDC (+- 5%)
- Supply Current 450 mA typ. at 50 MHz
- Size 82mm x 33mm

2 ADNP/ESC1 OVERVIEW



① U2 - Flash memory
② J2 - Byteblaster Active Serial mode
③ U3 - EP1C6F256 Cyclone FPGA
④ U8 - SDRAM
⑤ U1 - 10/100 Mbps Ethernet controller
⑥ J1 - 128-pin QIL connector

Figure 2-1: Overview ADNP/ESC1

3 ADNP/ESC1 COMPONENTS

This chapter describes the components of the DIL/NetPC ADNP/ESC1 shown in **chapter 2** and gives a short overview about their respective functions.

3.1 Flash Memory – U2

The 8MByte Flash memory works with a 16-bit data path and provides storage for the ADNP/ESC1 µClinux operating system with TCP/IP stack, Telnet server, file transfer utilities and an embedded Web server as well as OEM applications and data.

The Flash memory is in-system programmable over the serial interface. The ADNP/ESC1 in-system programming feature was developed to make it easier to update the on-board Flash content in the field.

3.2 Byteblaster Connector – J2

This connector can be used to connect the Altera Byteblaster adapter for the in-system programming of the Altera EP1C6F256 Cyclone FPGA. The interface uses a special transfer protocol called Active Serial Mode (AS–Mode). Please contact SSV for further information.

3.3 EP1C6F256 Cyclone FPGA – U3

The Altera EP1C6F256 Cyclone FPGA comes within a 256-pin FineLine BGA case and offers 6k logic elements for IP integration and proprietary code, 90 Kbits internal RAM, 2 PLLs, and up to 185 user I/Os.

The Cyclone FPGA implements the ADNP/ESC1 MCU (MicroController Unit) with a 32-bit RISC NIOS Softcore CPU with 512 internal registers, timers, two UARTs, 20-bit parallel I/O ports, SDRAM controller, Tri-State brigde and a SPI interface. The clock speed is 50 MHz.

3.4 SDRAM – U8

The capacity of the SDRAM memory chip is 16 MByte with a 32-bit data path.

3.5 10/100 Mbps Ethernet Controller – U1

The ADNP/ESC1 is using a SMSC 10/100Mbps LAN controller chip that allows Ethernet connectivity with a speed up to 100Mbps.

3.6 128-Pin QIL Connector – J1

The mechanical interface between the DIL/NetPC ADNP/ESC1 and existing devices and equipment is a 128-pin QIL (Quad- In- Line) connector with 2.54mm centers. This connector consist of four lines each with 32 pins.

Note: These pins are driven by an Altera EP1C6F256 Cyclone FPGA. It is possible to change the function of these pins. Please contact our support staff for more details.

Please refer to **chapter A2.1** for the complete pinout.

APPENDIX 1: MECHANICAL DIMENSIONS

The ADNP/ESC1 uses a 128-pin QIL socket as mechanical base. **Figure A1-1** shows the dimensions. All length dimensions have a tolerance of 0.5mm.

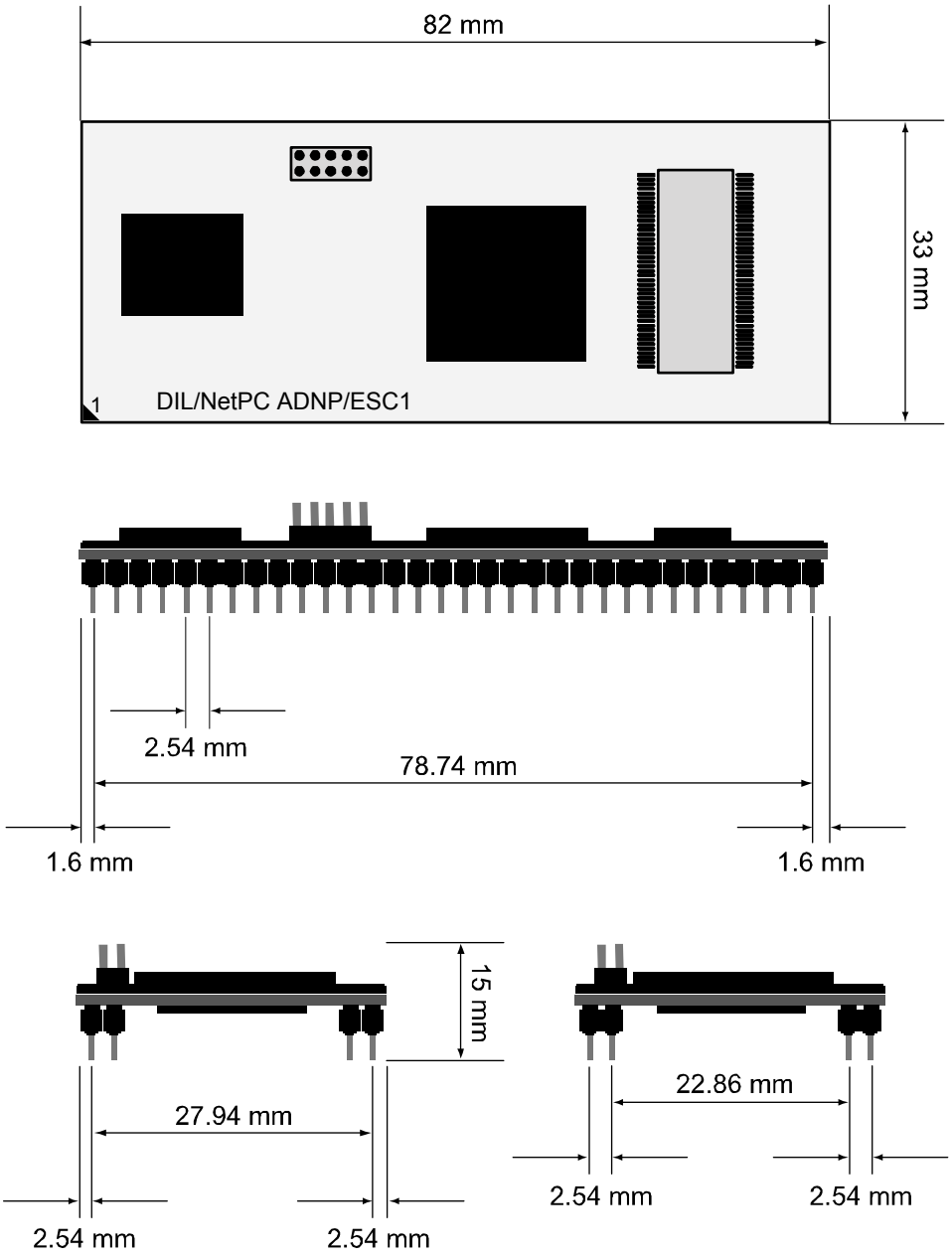


Figure A1-1: Mechanical dimensions of DNP/EVA7

APPENDIX 2: PIN ASSIGNMENT – 128-PIN QIL CONNECTOR

A2.1 Pin Assignment - 128-pin QIL Connector J1 (1. Part)

Pin	Name	Group	Function
1	PA0	PIO	Parallel I/O, Port A, Bit 0 (Driven by FPGA)
2	PA1	PIO	Parallel I/O, Port A, Bit 1 (Driven by FPGA)
3	PA2	PIO	Parallel I/O, Port A, Bit 2 (Driven by FPGA)
4	PA3	PIO	Parallel I/O, Port A, Bit 3 (Driven by FPGA)
5	PA4	PIO	Parallel I/O, Port A, Bit 4 (Driven by FPGA)
6	PA5	PIO	Parallel I/O, Port A, Bit 5 (Driven by FPGA)
7	PA6	PIO	Parallel I/O, Port A, Bit 6 (Driven by FPGA)
8	PA7	PIO	Parallel I/O, Port A, Bit 7 (Driven by FPGA)
9	PB0	PIO	Parallel I/O, Port B, Bit 0 (Driven by FPGA)
10	PB1	PIO	Parallel I/O, Port B, Bit 1 (Driven by FPGA)
11	PB2	PIO	Parallel I/O, Port B, Bit 2 (Driven by FPGA)
12	PB3	PIO	Parallel I/O, Port B, Bit 3 (Driven by FPGA)
13	PB4	PIO	Parallel I/O, Port B, Bit 4 (Driven by FPGA)
14	PB5	PIO	Parallel I/O, Port B, Bit 5 (Driven by FPGA)
15	PB6	PIO	Parallel I/O, Port B, Bit 6 (Driven by FPGA)
16	PB7	PIO	Parallel I/O, Port B, Bit 7 (Driven by FPGA)
17	PC0	PIO	Parallel I/O, Port C, Bit 0 (Driven by FPGA)
18	PC1	PIO	Parallel I/O, Port C, Bit 1 (Driven by FPGA)
19	PC2	PIO	Parallel I/O, Port C, Bit 2 (Driven by FPGA)
20	PC3	PIO	Parallel I/O, Port C, Bit 3 (Driven by FPGA)
21	RXD1	SIO	COM1 Serial Port, RXD PIN (Driven by FPGA)
22	TXD1	SIO	COM1 Serial Port, TXD PIN (Driven by FPGA)
23	CTS1	SIO	COM1 Serial Port, CTS PIN (Driven by FPGA)
24	RTS1	SIO	COM1 Serial Port, RTS PIN (Driven by FPGA)
25	DCD1	SIO	COM1 Serial Port, DCD PIN (Driven by FPGA)
26	DSR1	SIO	COM1 Serial Port, DSR PIN (Driven by FPGA)
27	DTR1	SIO	COM1 Serial Port, DTR PIN (Driven by FPGA)
28	RI1	SIO	COM1 Serial Port, RI PIN (Driven by FPGA)
29	RESIN	RESET	RESET Input
30	TX+	LAN	10/100 Mbps Ethernet Interface, TX+ Pin
31	TX-	LAN	10/100 Mbps Ethernet Interface, TX- Pin
32	GND	---	Ground

Table A2-1: 128-pin QIL connector pinout – pin 1 to 32

A2.2 Pin Assignment - 128-pin QIL Connector J1 (2. Part)

Pin	Name	Group	Function
33	RX+	LAN	10/100 Mbps Ethernet Interface, RX+ Pin
34	RX-	LAN	10/100 Mbps Ethernet Interface, RX- Pin
35	RESOUT	RESET	RESET Output
36	VBAT	PSP*	SC520 Real Time Clock Battery Input
37	CLKOUT	PSP*	Clock Output (Default 3.6864 MHz)
38	TXD2	PSP*	COM2 Serial Port, TXD Pin (Driven by FPGA)
39	RXD2	PSP*	COM2 Serial Port, RXD Pin (Driven by FPGA)
40	INT5	PSP*	Programmable Interrupt Input 5 (Driven by FPGA)
41	INT4	PSP*	Programmable Interrupt Input 4 (Driven by FPGA)
42	INT3	PSP*	Programmable Interrupt Input 3 (Driven by FPGA)
43	INT2	PSP*	Programmable Interrupt Input 2 (Driven by FPGA)
44	INT1	PSP*	Programmable Interrupt Input 1 (Driven by FPGA)
45	CS4	PSP*	Programmable Chip Select Output 4 (Driven by FPGA)
46	CS3	PSP*	Programmable Chip Select Output 3 (Driven by FPGA)
47	CS2	PSP*	Programmable Chip Select Output 2 (Driven by FPGA)
48	CS1	PSP*	Programmable Chip Select Output 1 (Driven by FPGA)
49	IOCHRDY	PSP*	I/O Channel Ready (Driven by FPGA)
50	IOR	PSP*	I/O Read Signal, I/O Expansion Bus (Driven by FPGA)
51	IOW	PSP*	I/O Write Signal, I/O Expansion Bus (Driven by FPGA)
52	SA3	PSP*	System Expansion Bus, Address Bit 3
53	SA2	PSP*	System Expansion Bus, Address Bit 2
54	SA1	PSP*	System Expansion Bus, Address Bit 1
55	SA0	PSP*	System Expansion Bus, Address Bit 0
56	SD7	PSP*	System Expansion Bus, Data Bit 7
57	SD6	PSP*	System Expansion Bus, Data Bit 6
58	SD5	PSP*	System Expansion Bus, Data Bit 5
59	SD4	PSP*	System Expansion Bus, Data Bit 4
60	SD3	PSP*	System Expansion Bus, Data Bit 3
61	SD2	PSP*	System Expansion Bus, Data Bit 2
62	SD1	PSP*	System Expansion Bus, Data Bit 1
63	SD0	PSP*	System Expansion Bus, Data Bit 0
64	Vcc	---	3.3 Volt Power Input
* = Product Specific Pins			

Table A2-2: 128-pin QIL connector pinout – pin 33 to 64

A2.3 Pin Assignment - 128-pin QIL Connector J1 (3. Part)

Pin	Name	Group	Function
65	SBHE	PSP*	System Byte High Enable, System Expansion Bus (Driven by FPGA)
66	IOCS16	PSP*	I/O Chip Select 16, System Expansion Bus (Driven by FPGA)
67	Reserved	PSP*	Reserved
68	Reserved	PSP*	Reserved
69	Reserved	PSP*	Reserved
70	BALE	PSP*	Bus Latch Enable, System Expansion Bus (Driven by FPGA)
71	AEN	PSP*	Address Enable Signal, System Expansion Bus (Driven by FPGA)
72	Reserved	PSP*	Reserved – Do not use
73	RCME	PSP*	Remote Console Mode Enable
74	Reserved	PSP*	Reserved – Do not use
75	Reserved	PSP*	Reserved – Do not use
76	Reserved	PSP*	Reserved – Do not use
77	Reserved	PSP*	Reserved – Do not use
78	Reserved	PSP*	Reserved – Do not use
79	Reserved	PSP*	Reserved – Do not use
80	Reserved	PSP*	Reserved – Do not use
81	Reserved	PSP*	Reserved – Do not use
82	Reserved	PSP*	Reserved – Do not use
83	Reserved	PSP*	Reserved – Do not use
84	Reserved	PSP*	Reserved – Do not use
85	INT6	PSP*	Programmable Interrupt Input 6 (Driven by FPGA)
86	INT7	PSP*	Programmable Interrupt Input 7 (Driven by FPGA)
87	IDERES	PSP*	IDE Interface Reset Output (Driven by FPGA)
88	IDECS0	PSP*	IDE Interface Chip Select 0 (Driven by FPGA)
89	IDECS1	PSP*	IDE Interface Chip Select 1 (Driven by FPGA)
90	Reserved	PSP*	Reserved – Do not use
91	Reserved	PSP*	Reserved – Do not use
92	Reserved	PSP*	Reserved – Do not use
93	Reserved	PSP*	Reserved – Do not use
94	Reserved	PSP*	Reserved – Do not use
95	Reserved	PSP*	Reserved – Do not use
96	GND	---	Ground
* = Product Specific Pins			

Table A2-3: 128-pin QIL connector pinout – pin 65 to 96

A2.4 Pin Assignment - 128-pin QIL Connector J1 (4. Part)

Pin	Name	Group	Function
97	LANLED	PSP*	LAN Interface Activty LED
98	Reserved	PSP*	Reserved – Do not use
99	RSTDRV	PSP*	Reset Output, System Expansion Bus (Driven by FPGA)
100	SA23	PSP*	System Expansion Bus, Address Bit 23
101	SA22	PSP*	System Expansion Bus, Address Bit 22
102	SA21	PSP*	System Expansion Bus, Address Bit 21
103	SA20	PSP*	System Expansion Bus, Address Bit 20
104	SA19	PSP*	System Expansion Bus, Address Bit 19
105	SA18	PSP*	System Expansion Bus, Address Bit 18
106	SA17	PSP*	System Expansion Bus, Address Bit 17
107	SA16	PSP*	System Expansion Bus, Address Bit 16
108	SA15	PSP*	System Expansion Bus, Address Bit 15
109	SA14	PSP*	System Expansion Bus, Address Bit 14
110	SA13	PSP*	System Expansion Bus, Address Bit 13
111	SA12	PSP*	System Expansion Bus, Address Bit 12
112	SA11	PSP*	System Expansion Bus, Address Bit 11
113	SA10	PSP*	System Expansion Bus, Address Bit 10
114	SA9	PSP*	System Expansion Bus, Address Bit 9
115	SA8	PSP*	System Expansion Bus, Address Bit 8
116	SA7	PSP*	System Expansion Bus, Address Bit 7
117	SA6	PSP*	System Expansion Bus, Address Bit 6
118	SA5	PSP*	System Expansion Bus, Address Bit 5
119	SA4	PSP*	System Expansion Bus, Address Bit 4
120	SD15	PSP*	System Expansion Bus, Data Bit 15
121	SD14	PSP*	System Expansion Bus, Data Bit 14
122	SD13	PSP*	System Expansion Bus, Data Bit 13
123	SD12	PSP*	System Expansion Bus, Data Bit 12
124	SD11	PSP*	System Expansion Bus, Data Bit 11
125	SD10	PSP*	System Expansion Bus, Data Bit 10
126	SD9	PSP*	System Expansion Bus, Data Bit 9
127	SD8	PSP*	System Expansion Bus, Data Bit 8
128	Vcc	---	3.3 Volt Power Input
* = Product Specific Pins			

Table A2-4: 128-pin QIL connector pinout – pin 97 to 128

Note: These pins are driven by a Altera EP1C6F256 Cyclone FPGA. It is possible to change the function of these pins. Please contact our support staff for more details.

APPENDIX 3: PIN ASSIGNMENT - BYTEBLASTER CONNECTOR

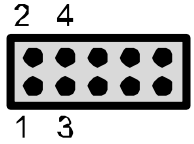
Top view	Pin	Name	Function
	1	DCLK	Clock
	2	GND	Ground
	3	CONF_DONE	Configuration Done
	4	Vcc3	Power
	5	nCONFIG	Configuration Control
	6	nCE	Cyclone Chip Enable
	7	DATAOUT	Active Serial Data Out
	8	nCS	Serial Config. Device Chip Select
	9	ASDI	Active Serial Data In
	10	GND	Ground

Table A3-1: Pinout Byteblaster connector

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1.0	2004-07-06	first version	WBU

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