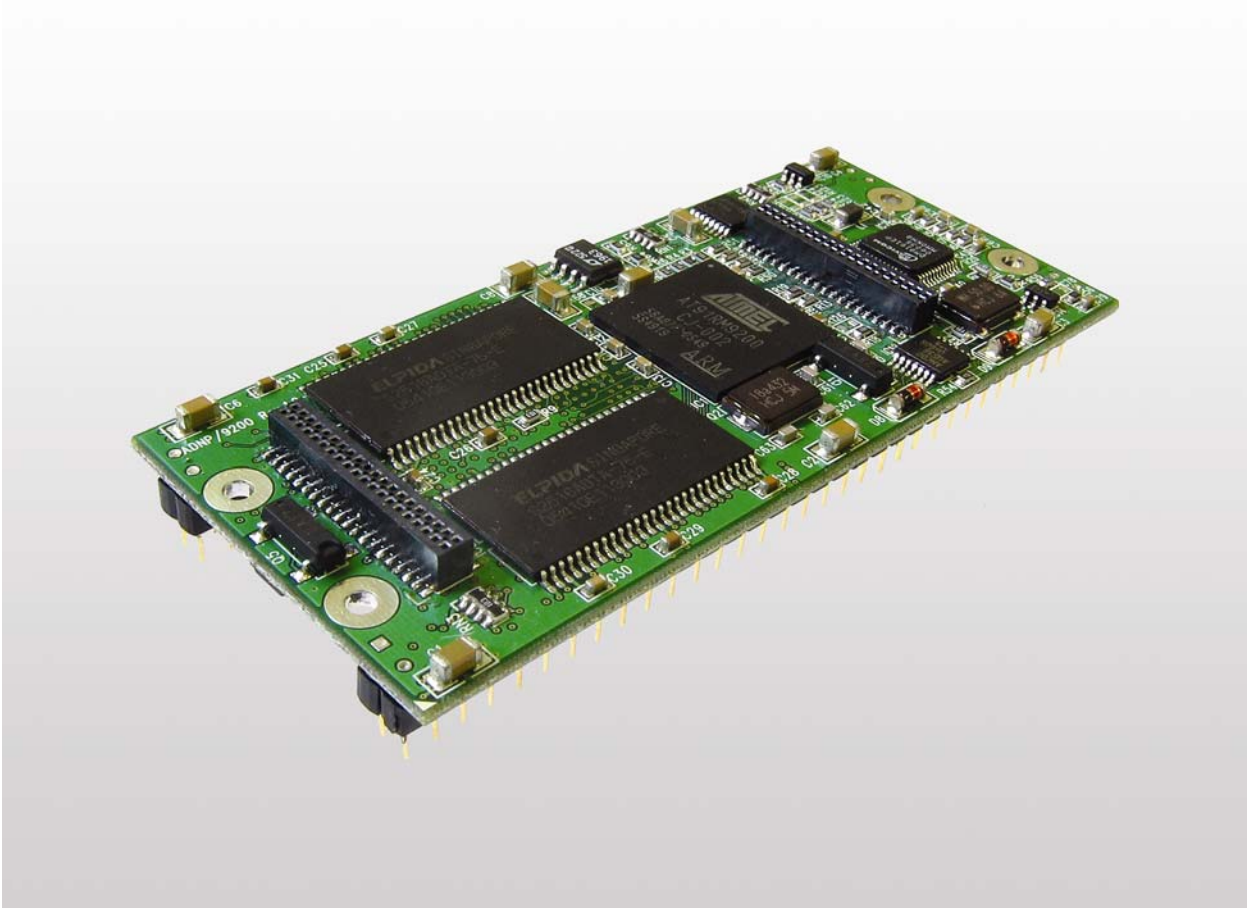
DIL/NetPC ADNP/9200
Board-Revision 1.0

Hardware Reference



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For further information regarding our products please visit us at www.dilnetpc.com

CONTENT

1 INTRODUCTION

This document describes the hardware components of the ADNP/9200. For further information about the individual components of this product you may follow the links from our website at `http://www.dilnetpc.com`.

Our website contains a lot of technical information, which will be updated in regular periods.

Figure 1 shows the block diagram of this small 32-bit embedded Linux computer.

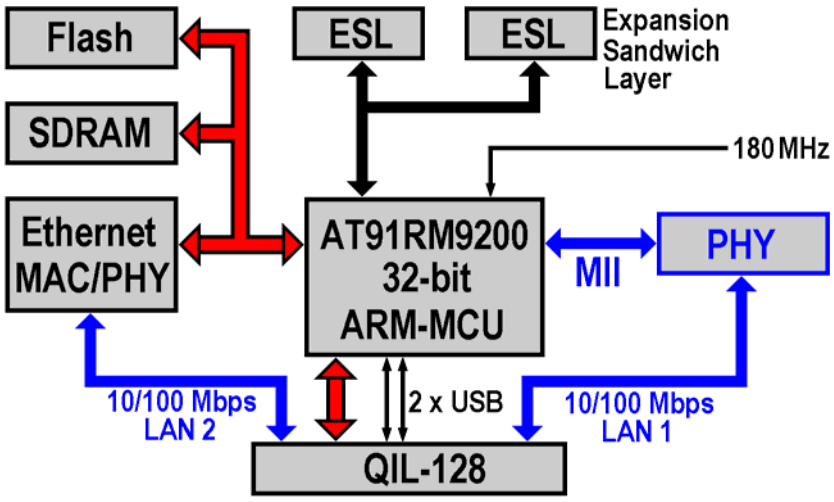


Figure 1: Block diagram of ADNP/9200

The ADNP/9200 is a ready-to-run embedded networking system. The use of the ADNP/9200 will allow you to realize a substantial time and costs saving over other chip-based approaches.

The ADNP/9200 comes with an Expansion Sandwich Layer (ESL) interface. This QIL-128-based DIL/NetPC has two connectors for small expansion boards, which allow sandwich layer solutions for wireless sensor network (WSN) interfaces. The ADNP/9200 works as gateway between TCP/IP-based Ethernet LANs and WSNs.

1.1 Features ADNP/9200

- 32-bit Atmel AT91RM9200 ARM MCU with 180 MHz clock speed
- 64 MByte SDRAM memory
- 16/32 MByte Flash memory
- 1 x 80-pin (Extension Sandwich Layer) connector
- 2 x 10/100 Mbps Ethernet interface
- 3 x serial port with TTL levels (1 x available via ESL)
- 1 x parallel port (20 bit + 8 bit via ESL)
- 1 x I/O extension bus (16 bit)
- 1 x USB device interface (on-board)
- 2 x USB host interface (on-board, 1 x via ESL)
- 3 x interrupt input
- 4 x programmable Chip Select output
- 1 x SPI interface
- Programmable Watchdog timer
- JTAG IEEE 1149.1 test interface (Multi-ICE compatible)
- In-System Programmable over JTAG, serial and Ethernet interface
- 128-pin QIL-connector with 2.54 mm centers
- 3.3 Volt low power design
- Supply voltage 3.3 VDC (±5 %)
- Size 82 x 36 mm

2 BOARD LAYOUT

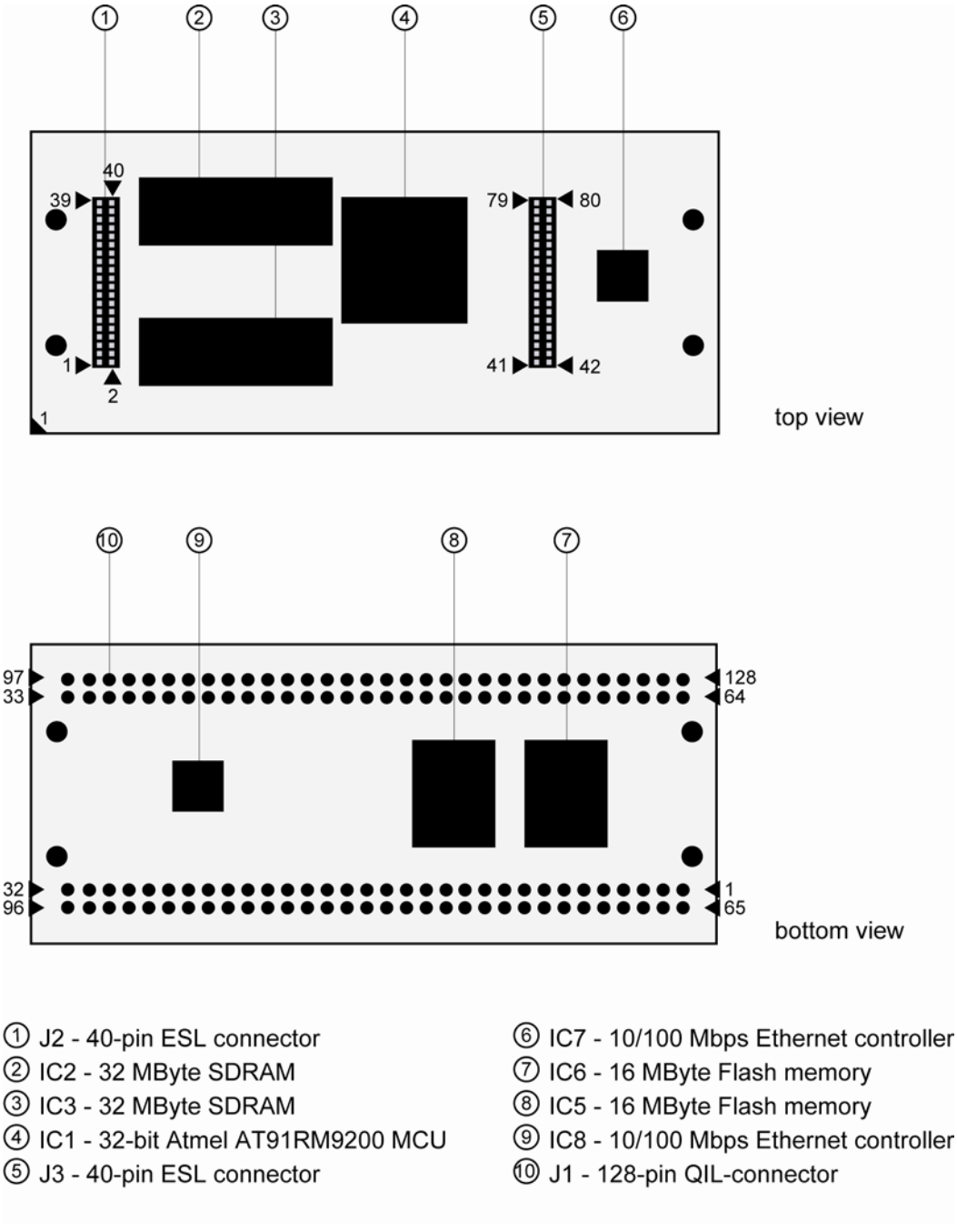


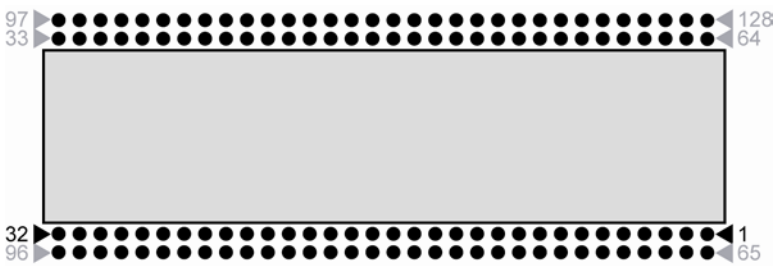
Figure 2: Board layout ADNP/9200

3 PINOUTS

3.1 128-pin QIL Connector (1. Part)

Pin	Name	Group	Function
1	PA0	PIO	Parallel I/O, Port A, Bit 0
2	PA1	PIO	Parallel I/O, Port A, Bit 1
3	PA2	PIO	Parallel I/O, Port A, Bit 2
4	PA3	PIO	Parallel I/O, Port A, Bit 3
5	PA4	PIO	Parallel I/O, Port A, Bit 4
6	PA5	PIO	Parallel I/O, Port A, Bit 5
7	PA6	PIO	Parallel I/O, Port A, Bit 6
8	PA7	PIO	Parallel I/O, Port A, Bit 7
9	PB0	PIO	Parallel I/O, Port B, Bit 0
10	PB1	PIO	Parallel I/O, Port B, Bit 1
11	PB2	PIO	Parallel I/O, Port B, Bit 2
12	PB3	PIO	Parallel I/O, Port B, Bit 3
13	PB4	PIO	Parallel I/O, Port B, Bit 4
14	PB5	PIO	Parallel I/O, Port B, Bit 5
15	PB6	PIO	Parallel I/O, Port B, Bit 6
16	PB7	PIO	Parallel I/O, Port B, Bit 7
17	PC0	PIO	Parallel I/O, Port C, Bit 0
18	PC1	PIO	Parallel I/O, Port C, Bit 1
19	PC2	PIO	Parallel I/O, Port C, Bit 2
20	PC3	PIO	Parallel I/O, Port C, Bit 3
21	RXD1	SIO	COM1 Serial Port, RXD Pin
22	TXD1	SIO	COM1 Serial Port, TXD Pin
23	CTS1	SIO	COM1 Serial Port, CTS Pin
24	RTS1	SIO	COM1 Serial Port, RTS Pin
25	DCD1	SIO	COM1 Serial Port, DCD Pin
26	DSR1	SIO	COM1 Serial Port, DSR Pin
27	DTR1	SIO	COM1 Serial Port, DTR Pin
28	RI1	SIO	COM1 Serial Port, RI Pin
29	RESIN	RESET	Reset Input
30	LAN1.TX+	LAN	10/100 Mbps Ethernet Interface 1, TX+ Pin
31	LAN1.TX-	LAN	10/100 Mbps Ethernet Interface 1, TX- Pin
32	GND	---	Ground

Table 1: 128-pin QIL connector pinout – pin 1 to 32

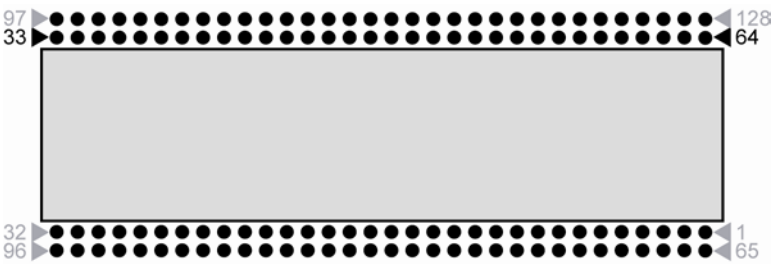


3.2 128-pin QIL Connector (2. Part)

Pin	Name	Group	Function
33	LAN1.RX+	LAN	10/100 Mbps Ethernet Interface 1, RX+ Pin
34	LAN1.RX-	LAN	10/100 Mbps Ethernet Interface 1, RX- Pin
35	RESOUT	RESET	Reset Output
36	VBAT	PSP*	Real Time Clock Battery Input
37	CLKOUT	PSP*	Clock Output (Default 1.8432 MHz)
38	TXD2	PSP*	COM2 Serial Port, TXD Pin
39	RXD2	PSP*	COM2 Serial Port, RXD Pin
40	HDM1	PSP*	USB Host 1 Port-
41	HDP1	PSP*	USB Host 1 Port+
42	DDM	PSP*	USB Device Port-
43	DDP	PSP*	USB Device Port+
44	INT1	PSP*	Programmable Interrupt Input 1
45	CS4	PSP*	Programmable Chip Select Output 4
46	CS3	PSP*	Programmable Chip Select Output 3
47	CS2	PSP*	Programmable Chip Select Output 2
48	CS1	PSP*	Programmable Chip Select Output 1
49	IOCHRDY	PSP*	I/O Channel Ready
50	IOR	PSP*	I/O Read Signal, I/O Expansion Bus
51	IOW	PSP*	I/O Write Signal, I/O Expansion Bus
52	SA3	PSP*	System Expansion Bus, Address Bit 3
53	SA2	PSP*	System Expansion Bus, Address Bit 2
54	SA1	PSP*	System Expansion Bus, Address Bit 1
55	SA0	PSP*	System Expansion Bus, Address Bit 0
56	SD7	PSP*	System Expansion Bus, Data Bit 7
57	SD6	PSP*	System Expansion Bus, Data Bit 6
58	SD5	PSP*	System Expansion Bus, Data Bit 5
59	SD4	PSP*	System Expansion Bus, Data Bit 4
60	SD3	PSP*	System Expansion Bus, Data Bit 3
61	SD2	PSP*	System Expansion Bus, Data Bit 2
62	SD1	PSP*	System Expansion Bus, Data Bit 1
63	SD0	PSP*	System Expansion Bus, Data Bit 0
64	Vcc	---	3.3 Volt Power Input

* = Product Specific Pins

Table 2: 128-pin QIL connector pinout – pin 33 to 64

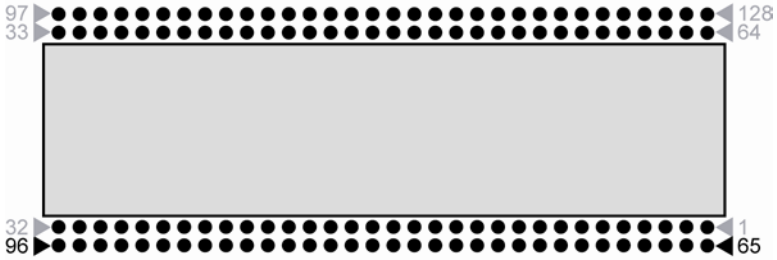


3.3 128-pin QIL Connector (3. Part)

Pin	Name	Group	Function
65	Reserved	---	Reserved – Do not use
66	Reserved	---	Reserved – Do not use
67	Reserved	---	Reserved – Do not use
68	Reserved	---	Reserved – Do not use
69	Reserved	---	Reserved – Do not use
70	Reserved	---	Reserved – Do not use
71	Reserved	---	Reserved – Do not use
72	Reserved	---	Reserved – Do not use
73	RCME	PSP*	Remote Console Mode Enable
74	TDI	PSP*	Test Data In
75	TDO	PSP*	Test Data Out
76	TMS#	PSP*	Test Mode Select
77	TCK	PSP*	Test Clock
78	TRST#	PSP*	Test Reset
79	WDDIS#	PSP*	Watchdog Disable
80	Reserved	---	Reserved – Do not use
81	Reserved	---	Reserved – Do not use
82	Reserved	---	Reserved – Do not use
83	Reserved	---	Reserved – Do not use
84	Reserved	---	Reserved – Do not use
85	INT6	PSP*	Programmable Interrupt Input 6
86	INT7	PSP*	Programmable Interrupt Input 7
87	Reserved	---	Reserved – Do not use
88	Reserved	---	Reserved – Do not use
89	Reserved	---	Reserved – Do not use
90	Reserved	---	Reserved – Do not use
91	Reserved	---	Reserved – Do not use
92	LAN2.TX+	PSP*	10/100 Mbps Ethernet Interface 2, TX+ Pin
93	LAN2.TX-	PSP*	10/100 Mbps Ethernet Interface 2, TX- Pin
94	LAN2.RX+	PSP*	10/100 Mbps Ethernet Interface 2, RX+ Pin
95	LAN2.RX-	PSP*	10/100 Mbps Ethernet Interface 2, RX- Pin
96	GND	---	Ground

* = Product Specific Pins

Table 3: 128-pin QIL connector pinout – pin 65 to 96

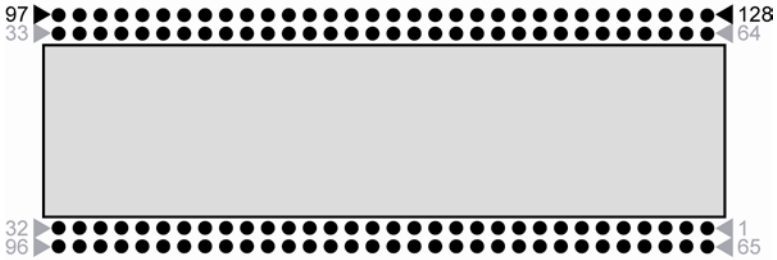


3.4 128-pin QIL Connector (4. Part)

Pin	Name	Group	Function
97	LAN1.LED	PSP*	LAN1 Interface Activity LED
98	LAN2.LED	PSP*	LAN2 Interface Activity LED
99	Reserved	---	Reserved – Do not use
100	SA23	PSP*	System Expansion Bus, Address Bit 23
101	SA22	PSP*	System Expansion Bus, Address Bit 22
102	SA21	PSP*	System Expansion Bus, Address Bit 21
103	SA20	PSP*	System Expansion Bus, Address Bit 20
104	SA19	PSP*	System Expansion Bus, Address Bit 19
105	SA18	PSP*	System Expansion Bus, Address Bit 18
106	SA17	PSP*	System Expansion Bus, Address Bit 17
107	SA16	PSP*	System Expansion Bus, Address Bit 16
108	SA15	PSP*	System Expansion Bus, Address Bit 15
109	SA14	PSP*	System Expansion Bus, Address Bit 14
110	SA13	PSP*	System Expansion Bus, Address Bit 13
111	SA12	PSP*	System Expansion Bus, Address Bit 12
112	SA11	PSP*	System Expansion Bus, Address Bit 11
113	SA10	PSP*	System Expansion Bus, Address Bit 10
114	SA9	PSP*	System Expansion Bus, Address Bit 9
115	SA8	PSP*	System Expansion Bus, Address Bit 8
116	SA7	PSP*	System Expansion Bus, Address Bit 7
117	SA6	PSP*	System Expansion Bus, Address Bit 6
118	SA5	PSP*	System Expansion Bus, Address Bit 5
119	SA4	PSP*	System Expansion Bus, Address Bit 4
120	SD15	PSP*	System Expansion Bus, Data Bit 15
121	SD14	PSP*	System Expansion Bus, Data Bit 14
122	SD13	PSP*	System Expansion Bus, Data Bit 13
123	SD12	PSP*	System Expansion Bus, Data Bit 12
124	SD11	PSP*	System Expansion Bus, Data Bit 11
125	SD10	PSP*	System Expansion Bus, Data Bit 10
126	SD9	PSP*	System Expansion Bus, Data Bit 9
127	SD8	PSP*	System Expansion Bus, Data Bit 8
128	Vcc	---	3.3 Volt Power Input

* = Product Specific Pins

Table 4: 128-pin QIL connector pinout – pin 97 to 128



3.5 80-pin ESL Connector (1. Part)

Pin	Name	Function
1	Vcc	3.3 Volt Power Input
2	GND	Ground
3	Reserved	Reserved – Do not use
4	Reserved	Reserved – Do not use
5	Reserved	Reserved – Do not use
6	Reserved	Reserved – Do not use
7	Vcc	3.3 Volt Power Input
8	GND	Ground
9	Reserved	Reserved – Do not use
10	Reserved	Reserved – Do not use
11	Reserved	Reserved – Do not use
12	Reserved	Reserved – Do not use
13	Reserved	Reserved – Do not use
14	Reserved	Reserved – Do not use
15	Reserved	Reserved – Do not use
16	Reserved	Reserved – Do not use
17	GND	Ground
18	Vcc	3.3 Volt Power Input
19	Reserved	Reserved – Do not use
20	RTS	Serial Port, RTS Pin
21	Reserved	Reserved – Do not use
22	TXD	Serial Port, TXD Pin
23	Reserved	Reserved – Do not use
24	RXD	Serial Port, RXD Pin
25	Reserved	Reserved – Do not use
26	CTS	Serial Port, CTS Pin
27	GND	Ground
28	Vcc	3.3 Volt Power Input
29	GPIO0	General Purpose I/O, Bit 0
30	GPIO1	General Purpose I/O, Bit 1
31	GPIO2	General Purpose I/O, Bit 2
32	GPIO3	General Purpose I/O, Bit 3
33	GPIO4	General Purpose I/O, Bit 4
34	GPIO5	General Purpose I/O, Bit 5
35	GPIO6	General Purpose I/O, Bit 6
36	GPIO7	General Purpose I/O, Bit 7
37	GND	Ground
38	GND	Ground
39	Vcc	3.3 Volt Power Input
40	Vcc	3.3 Volt Power Input

Table 5: 80-pin ESL connector pinout – pin 1 to 40

3.6 80-pin ESL Connector (2. Part)

Pin	Name	Function
41	Vcc	3.3 Volt Power Input
42	Vcc	3.3 Volt Power Input
43	GND	Ground
44	GND	Ground
45	Reserved	Reserved – Do not use
46	Reserved	Reserved – Do not use
47	Reserved	Reserved – Do not use
48	Reserved	Reserved – Do not use
49	GND	Ground
50	GND	Ground
51	Reserved	Reserved – Do not use
52	Reserved	Reserved – Do not use
53	Vcc	3.3 Volt Power Input
54	GND	Ground
55	Reserved	Reserved – Do not use
56	Reserved	Reserved – Do not use
57	Reserved	Reserved – Do not use
58	Reserved	Reserved – Do not use
59	Reserved	Reserved – Do not use
60	Reserved	Reserved – Do not use
61	Reserved	Reserved – Do not use
62	Reserved	Reserved – Do not use
63	Vcc	3.3 Volt Power Input
64	GND	Ground
65	PC0	Parallel I/O, Port C, Bit 0, SPI MOSI
66	Reserved	Reserved – Do not use
67	PC1	Parallel I/O, Port C, Bit 1, SPI MISO
68	Reserved	Reserved – Do not use
69	PC2	Parallel I/O, Port C, Bit 2, SPI SPCK
70	Reserved	Reserved – Do not use
71	PC3	Parallel I/O, Port C, Bit 3, SPI Chip Select 0
72	Reserved	Reserved – Do not use
73	GND	Ground
74	Vcc	3.3 Volt Power Input
75	HDP2	USB Host 2 Port+
76	Reserved	Reserved – Do not use
77	HDM2	USB Host 2 Port-
78	Reserved	Reserved – Do not use
79	GND	Ground
80	Vcc	3.3 Volt Power Input

Table 6: 80-pin ESL connector pinout – pin 41 to 80

3.7 JTAG Interface

The JTAG signals of the ADNP/9200 QIL-128 connector are directly connected to the JTAG TAP controller of the AT91RM9200 32-bit ARM-MCU.

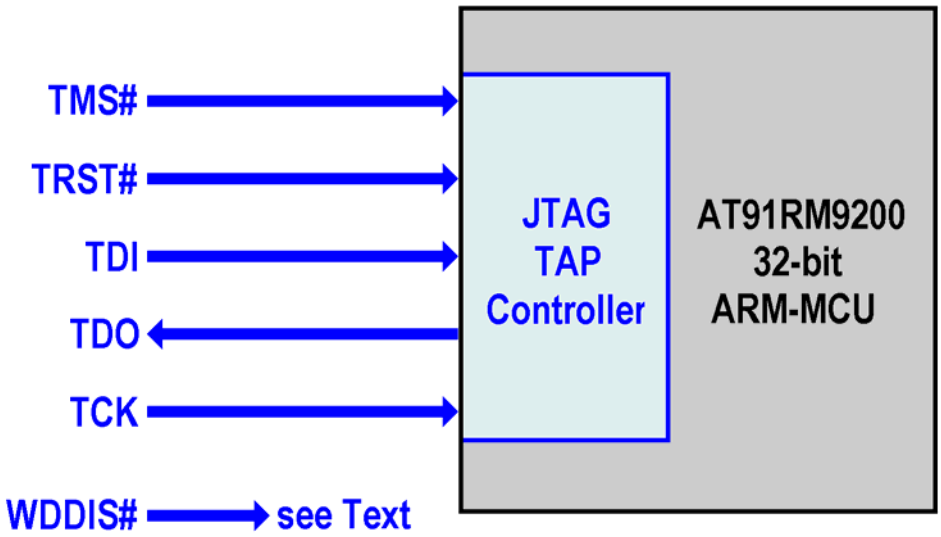


Figure 3: ADNP/9200 JTAG interface

The WDDIS# input disables the on-board watchdog. This is necessary to access the Flash chips over JTAG programming tools.

4 MECHANICAL DIMENSIONS

All length dimensions have a tolerance of 0.5 mm. The drillings are suitable for M2 screws.

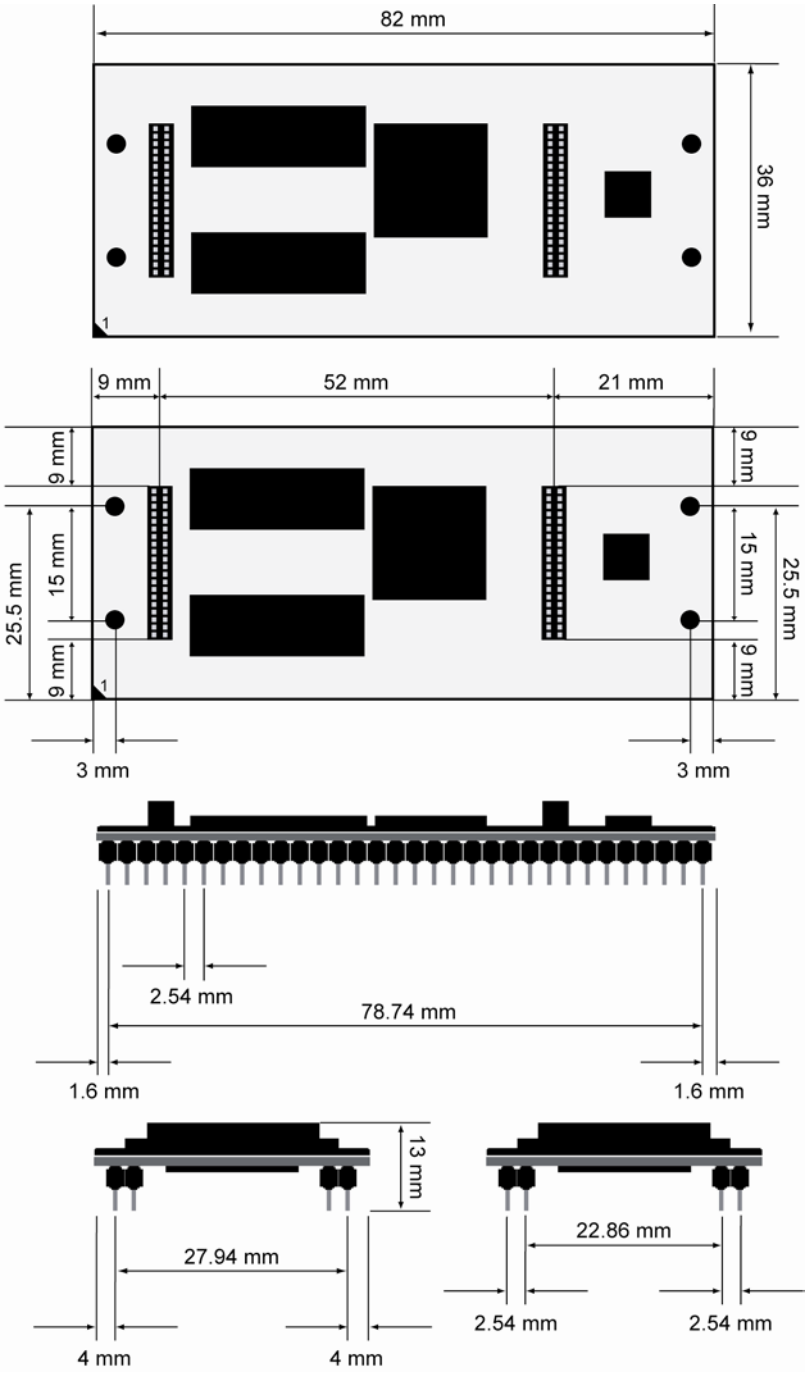


Figure 4: Mechanical dimensions of ADNP/9200

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DOCUMENT HISTORY

Revision	Date	Remarks	Name
0.1	2006-05-08	first version	WBU
0.2	2006-08-07	small errors corrected	WBU

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