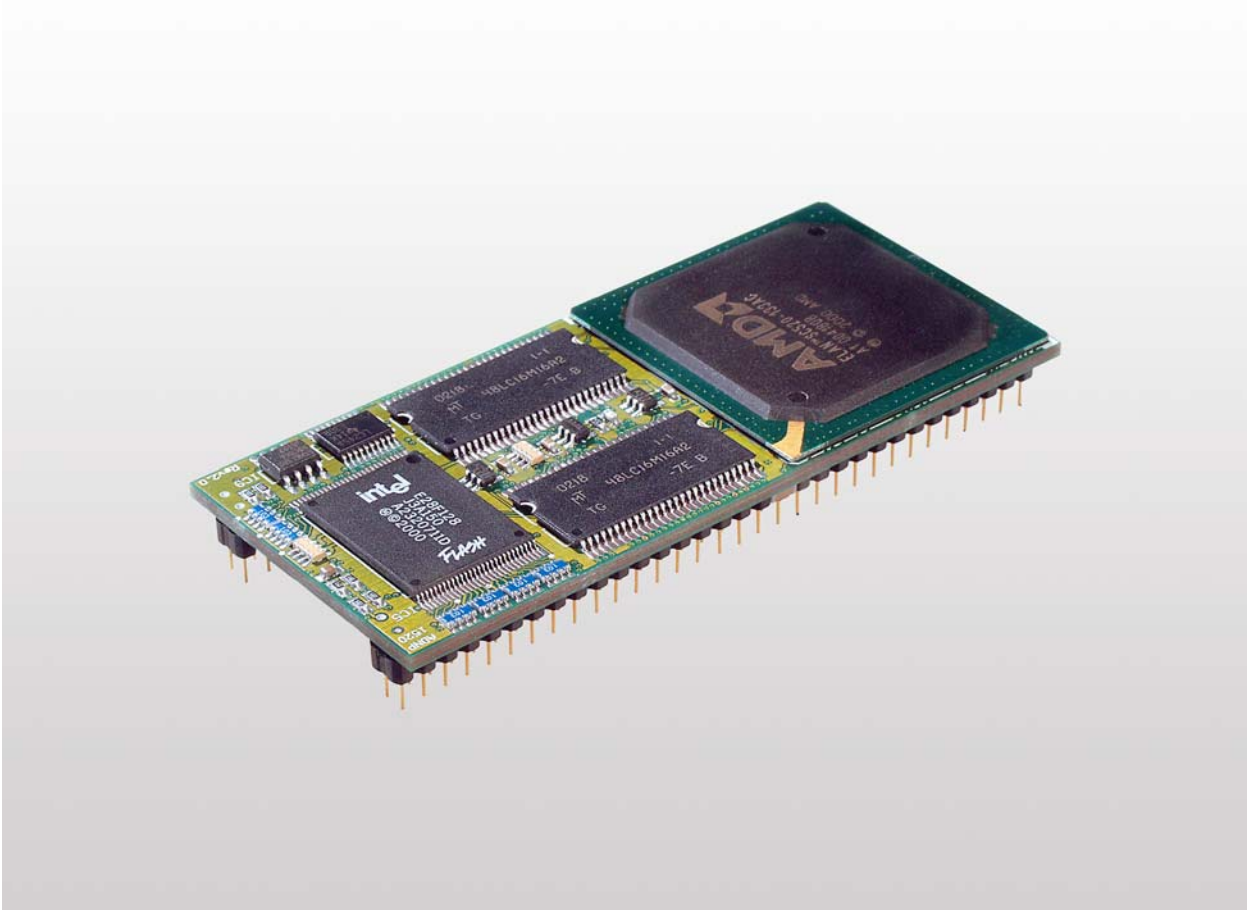
DIL/NetPC ADNP/1520
Board Revision 2.1

Hardware Reference



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For further information regarding our products please visit us at www.dilnetpc.com

CONTENT

1 INTRODUCTION

This document describes the hardware components of the ADNP/1520. For further information about the individual components of this product you may follow the links from the website at http://www.dilnetpc.com. This website contains a lot of technical information, which will be updated in regular periods. Figure 1 shows the block diagram of this small 32-bit embedded Linux computer.

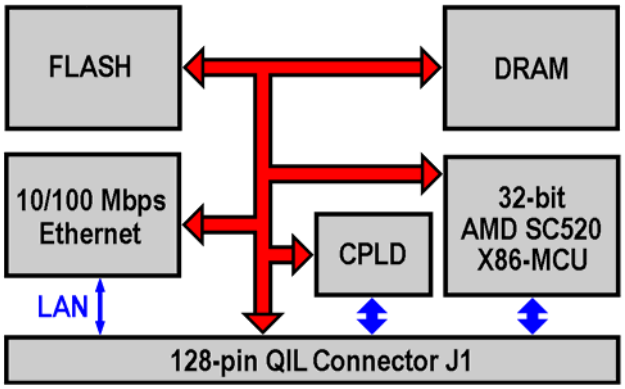


Figure 1: Block diagram of ADNP/1520

The DIL/NetPC ADNP/1520 is an upgrade to the ADNP/1486 and DNP/1486. This DIL/NetPC offers a footprint of the ADNP/1486 128-pin QIL (Quad-In-Line) socket with 2.54 mm centers. The inner 64 pins are compatible to the DIL/NetPC DNP/1486 and other DIL-64 devices. The outer 64 pins offer a 16-bit ISA expansion bus.

The DIL/NetPC ADNP/1520 was developed specifically for OEM products and subsystems that need to be connected to TCP/IP-based 10/100 Mbps Ethernet networks with minimum development costs.

The ADNP/1520 is a ready-to-run embedded networking system. The use of the ADNP/1520 will allow you to realize a substantial time and costs savings over other chip-based approaches.

1.1 Features ADNP/1520

- AMD 32-bit SC520 Low Power IA-32 586 CPU with 133 MHz Clock Speed
- Hardware FPU (Floating Point Unit) ANSI/IEEE 754 compliant
- 64 MByte SDRAM Memory
- 16 MByte Boot Block Flash Memory
- 10/100 Mbps Ethernet Interface
- COM1/COM2 16550 Serial Ports with TTL Levels
- High density PLD (CPLD) for VHDL programming
- 20-bit General Purpose Parallel I/O (VHDL-based, driven by CPLD)
- Programmable Watchdog Timer
- 16-bit ISA Expansion Bus
- Seven Interrupt Inputs
- Four programmable Chip Select Outputs
- IDE Interface
- JTAG IEEE 1149.1 Test Interface
- 128-pin QIL-Connector with 2.54 mm Centers
- In-System Programmable over JTAG, serial and Ethernet Interface
- 3.3 Volt Low Power Design
- Supply Voltage 3.3 VDC (±5 %)
- Supply Current 350 mA typ. (950 mA max.)
- Size 82 x 36 mm

2 BOARD LAYOUT

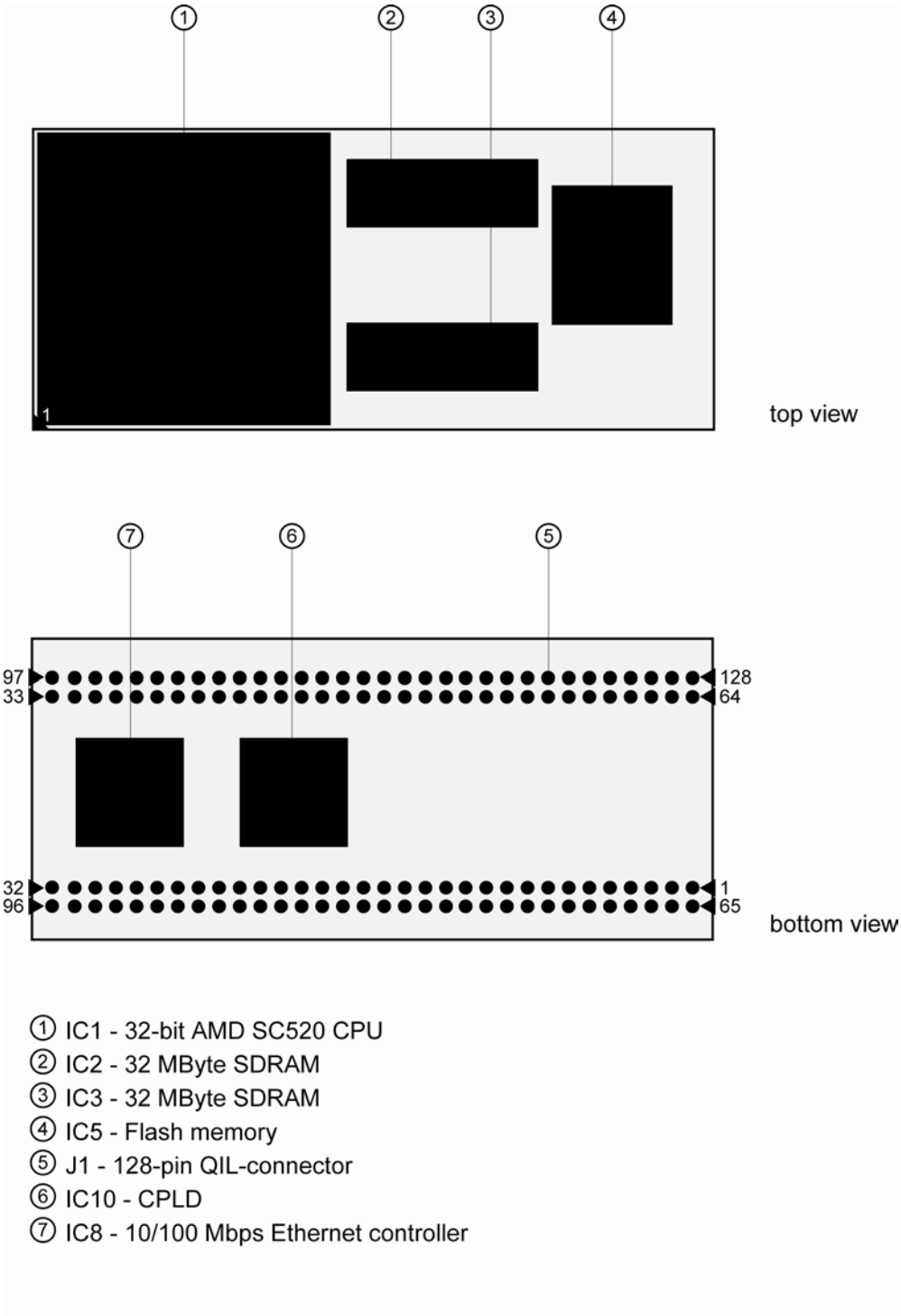


Figure 2: Board layout ADNP/1520

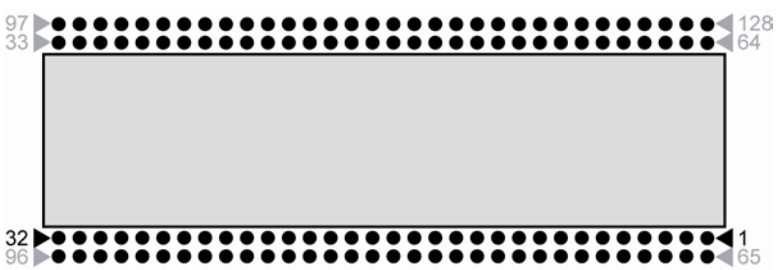
3 PINOUTS

3.1 128-pin QIL Connector (1. Part)

Pin	Name	Group	Function
1	PA0	PIO	Parallel I/O, Port A, Bit 0 *
2	PA1	PIO	Parallel I/O, Port A, Bit 1 *
3	PA2	PIO	Parallel I/O, Port A, Bit 2 *
4	PA3	PIO	Parallel I/O, Port A, Bit 3 *
5	PA4	PIO	Parallel I/O, Port A, Bit 4 *
6	PA5	PIO	Parallel I/O, Port A, Bit 5 *
7	PA6	PIO	Parallel I/O, Port A, Bit 6 *
8	PA7	PIO	Parallel I/O, Port A, Bit 7 *
9	PB0	PIO	Parallel I/O, Port B, Bit 0 *
10	PB1	PIO	Parallel I/O, Port B, Bit 1 *
11	PB2	PIO	Parallel I/O, Port B, Bit 2 *
12	PB3	PIO	Parallel I/O, Port B, Bit 3 *
13	PB4	PIO	Parallel I/O, Port B, Bit 4 *
14	PB5	PIO	Parallel I/O, Port B, Bit 5 *
15	PB6	PIO	Parallel I/O, Port B, Bit 6 *
16	PB7	PIO	Parallel I/O, Port B, Bit 7 *
17	PC0	PIO	Parallel I/O, Port C, Bit 0 *
18	PC1	PIO	Parallel I/O, Port C, Bit 1 *
19	PC2	PIO	Parallel I/O, Port C, Bit 2 *
20	PC3	PIO	Parallel I/O, Port C, Bit 3 *
21	RXD1	SIO	COM1 Serial Port, RXD Pin
22	TXD1	SIO	COM1 Serial Port, TXD Pin
23	CTS1	SIO	COM1 Serial Port, CTS Pin
24	RTS1	SIO	COM1 Serial Port, RTS Pin
25	DCD1	SIO	COM1 Serial Port, DCD Pin
26	DSR1	SIO	COM1 Serial Port, DSR Pin
27	DTR1	SIO	COM1 Serial Port, DTR Pin
28	RI1	SIO	COM1 Serial Port, RI Pin
29	RESIN	RESET	RESET Input
30	TX+	LAN	10/100 Mbps Ethernet Interface, TX+ Pin
31	TX-	LAN	10/100 Mbps Ethernet Interface, TX- Pin
32	GND	---	Ground

***Please note:** The PIO pins 1 to 20 are driven by an in-system programmable (ISP) high density PLD (ispMACH4256 or similar). It is possible to change the function of these pins over the ADNP/1520 JTAG interface. Please contact our support staff for more details.

Table 1: 128-pin QIL connector pinout – pin 1 to 32

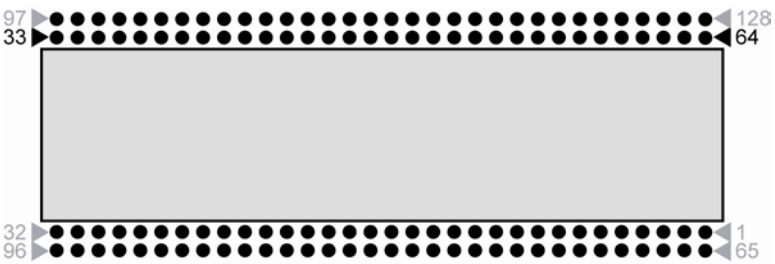


3.2 128-pin QIL Connector (2. Part)

Pin	Name	Group	Function
33	RX+	LAN	10/100 Mbps Ethernet Interface, RX+ Pin
34	RX-	LAN	10/100 Mbps Ethernet Interface, RX- Pin
35	RESOUT	RESET	RESET Output
36	VBAT	PSP*	Real Time Clock Battery Input
37	CLKOUT	PSP*	Clock Output (Default 1.8432 MHz)
38	TXD2	PSP*	COM2 Serial Port, TXD Pin
39	RXD2	PSP*	COM2 Serial Port, RXD Pin
40	INT5	PSP*	Programmable Interrupt Input 5
41	INT4	PSP*	Programmable Interrupt Input 4
42	INT3	PSP*	Programmable Interrupt Input 3
43	INT2	PSP*	Programmable Interrupt Input 2
44	INT1	PSP*	Programmable Interrupt Input 1
45	CS4	PSP*	Programmable Chip Select Output 4
46	CS3	PSP*	Programmable Chip Select Output 3
47	CS2	PSP*	Programmable Chip Select Output 2
48	CS1	PSP*	Programmable Chip Select Output 1
49	IOCHRD	PSP*	I/O Channel Ready
50	IOR	PSP*	I/O Read Signal, I/O Expansion Bus
51	IOW	PSP*	I/O Write Signal, I/O Expansion Bus
52	SA3	PSP*	System Expansion Bus, Address Bit 3
53	SA2	PSP*	System Expansion Bus, Address Bit 2
54	SA1	PSP*	System Expansion Bus, Address Bit 1
55	SA0	PSP*	System Expansion Bus, Address Bit 0
56	SD7	PSP*	System Expansion Bus, Data Bit 7
57	SD6	PSP*	System Expansion Bus, Data Bit 6
58	SD5	PSP*	System Expansion Bus, Data Bit 5
59	SD4	PSP*	System Expansion Bus, Data Bit 4
60	SD3	PSP*	System Expansion Bus, Data Bit 3
61	SD2	PSP*	System Expansion Bus, Data Bit 2
62	SD1	PSP*	System Expansion Bus, Data Bit 1
63	SD0	PSP*	System Expansion Bus, Data Bit 0
64	Vcc	---	3.3 Volt Power Input

* = Product Specific Pins

Table 2: 128-pin QIL connector pinout – pin 33 to 64

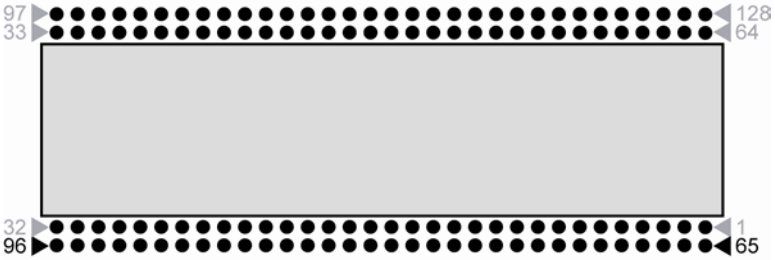


3.3 128-pin QIL Connector (3. Part)

Pin	Name	Group	Function
65	SBHE	PSP*	System Byte High Enable, System Expansion Bus
66	IOCS16	PSP*	I/O Chip Select 16, System Expansion Bus
67	MEMCS	PSP*	Memory Chip Select 16, System Expansion Bus
68	MEMW	PSP*	Memory Write Signal, System Expansion Bus
69	MEMR	PSP*	Memory Read Signal, System Expansion Bus
70	BALE	PSP*	Bus Latch Enable, System Expansion Bus
71	AEN	PSP*	Address Enable Signal, System Expansion Bus
72	Reserved	PSP*	Reserved – Do not use
73	RCME	PSP*	Remote Console Mode Enable
74	Reserved	PSP*	Reserved – Do not use
75	Reserved	PSP*	Reserved – Do not use
76	Reserved	PSP*	Reserved – Do not use
77	Reserved	PSP*	Reserved – Do not use
78	Reserved	PSP*	Reserved – Do not use
79	Reserved	PSP*	Reserved – Do not use
80	Reserved	PSP*	Reserved – Do not use
81	Reserved	PSP*	Reserved – Do not use
82	Reserved	PSP*	Reserved – Do not use
83	Reserved	PSP*	Reserved – Do not use
84	Reserved	PSP*	Reserved – Do not use
85	INT6	PSP*	Programmable Interrupt Input 6
86	INT7	PSP*	Programmable Interrupt Input 7
87	IDERES	PSP*	IDE Interface Reset Output
88	IDECS0	PSP*	IDE Interface Chip Select 0
89	IDECS1	PSP*	IDE Interface Chip Select 1
90	Reserved	PSP*	Reserved – Do not use
91	Reserved	PSP*	Reserved – Do not use
92	Reserved	PSP*	Reserved – Do not use
93	Reserved	PSP*	Reserved – Do not use
94	Reserved	PSP*	Reserved – Do not use
95	Reserved	PSP*	Reserved – Do not use
96	GND	---	Ground

* = Product Specific Pins

Table 3: 128-pin QIL connector pinout – pin 65 to 96

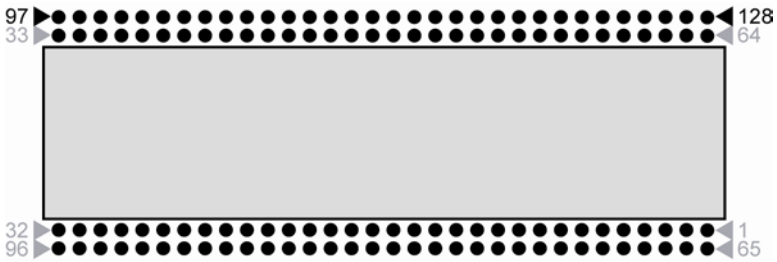


3.4 128-pin QIL Connector (4. Part)

Pin	Name	Group	Function
97	LANLED	PSP*	LAN Interface Activity LED
98	Reserved	PSP*	Reserved – Do not use
99	RSTDRV	PSP*	Reset Output, System Expansion Bus
100	SA23	PSP*	System Expansion Bus, Address Bit 23
101	SA22	PSP*	System Expansion Bus, Address Bit 22
102	SA21	PSP*	System Expansion Bus, Address Bit 21
103	SA20	PSP*	System Expansion Bus, Address Bit 20
104	SA19	PSP*	System Expansion Bus, Address Bit 19
105	SA18	PSP*	System Expansion Bus, Address Bit 18
106	SA17	PSP*	System Expansion Bus, Address Bit 17
107	SA16	PSP*	System Expansion Bus, Address Bit 16
108	SA15	PSP*	System Expansion Bus, Address Bit 15
109	SA14	PSP*	System Expansion Bus, Address Bit 14
110	SA13	PSP*	System Expansion Bus, Address Bit 13
111	SA12	PSP*	System Expansion Bus, Address Bit 12
112	SA11	PSP*	System Expansion Bus, Address Bit 11
113	SA10	PSP*	System Expansion Bus, Address Bit 10
114	SA9	PSP*	System Expansion Bus, Address Bit 9
115	SA8	PSP*	System Expansion Bus, Address Bit 8
116	SA7	PSP*	System Expansion Bus, Address Bit 7
117	SA6	PSP*	System Expansion Bus, Address Bit 6
118	SA5	PSP*	System Expansion Bus, Address Bit 5
119	SA4	PSP*	System Expansion Bus, Address Bit 4
120	SD15	PSP*	System Expansion Bus, Data Bit 15
121	SD14	PSP*	System Expansion Bus, Data Bit 14
122	SD13	PSP*	System Expansion Bus, Data Bit 13
123	SD12	PSP*	System Expansion Bus, Data Bit 12
124	SD11	PSP*	System Expansion Bus, Data Bit 11
125	SD10	PSP*	System Expansion Bus, Data Bit 10
126	SD9	PSP*	System Expansion Bus, Data Bit 9
127	SD8	PSP*	System Expansion Bus, Data Bit 8
128	Vcc	---	3.3 Volt Power Input

* = Product Specific Pins

Table 4: 128-pin QIL connector pinout – pin 97 to 128



4 MECHANICAL DIMENSIONS

All length dimensions have a tolerance of 0.5 mm.

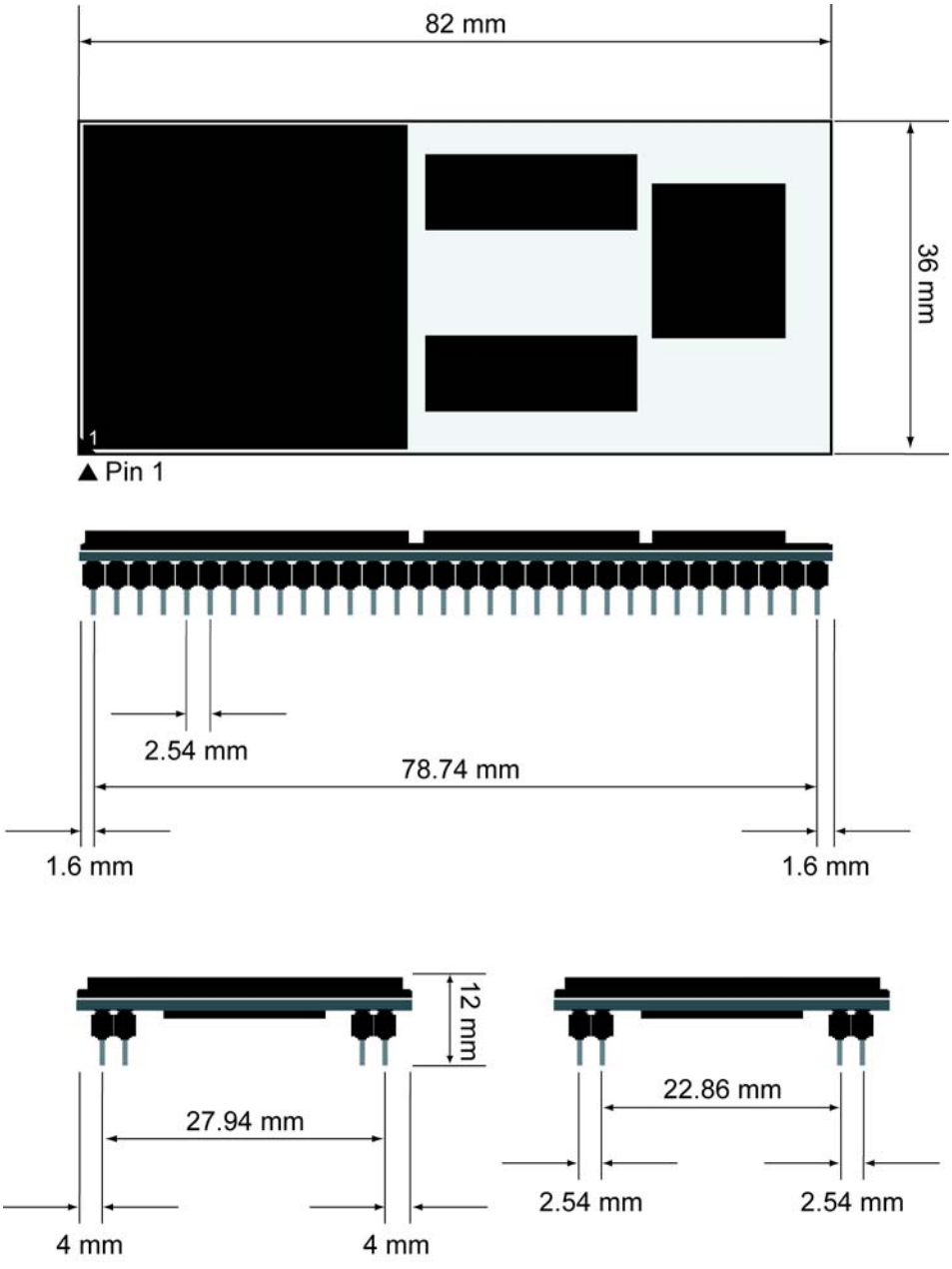


Figure 3: Mechanical dimensions of ADNP/1520

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1.0	2005-06-29	First version	WBU
1.1	2006-01-24	New figure 1 and figure 2	KDW

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